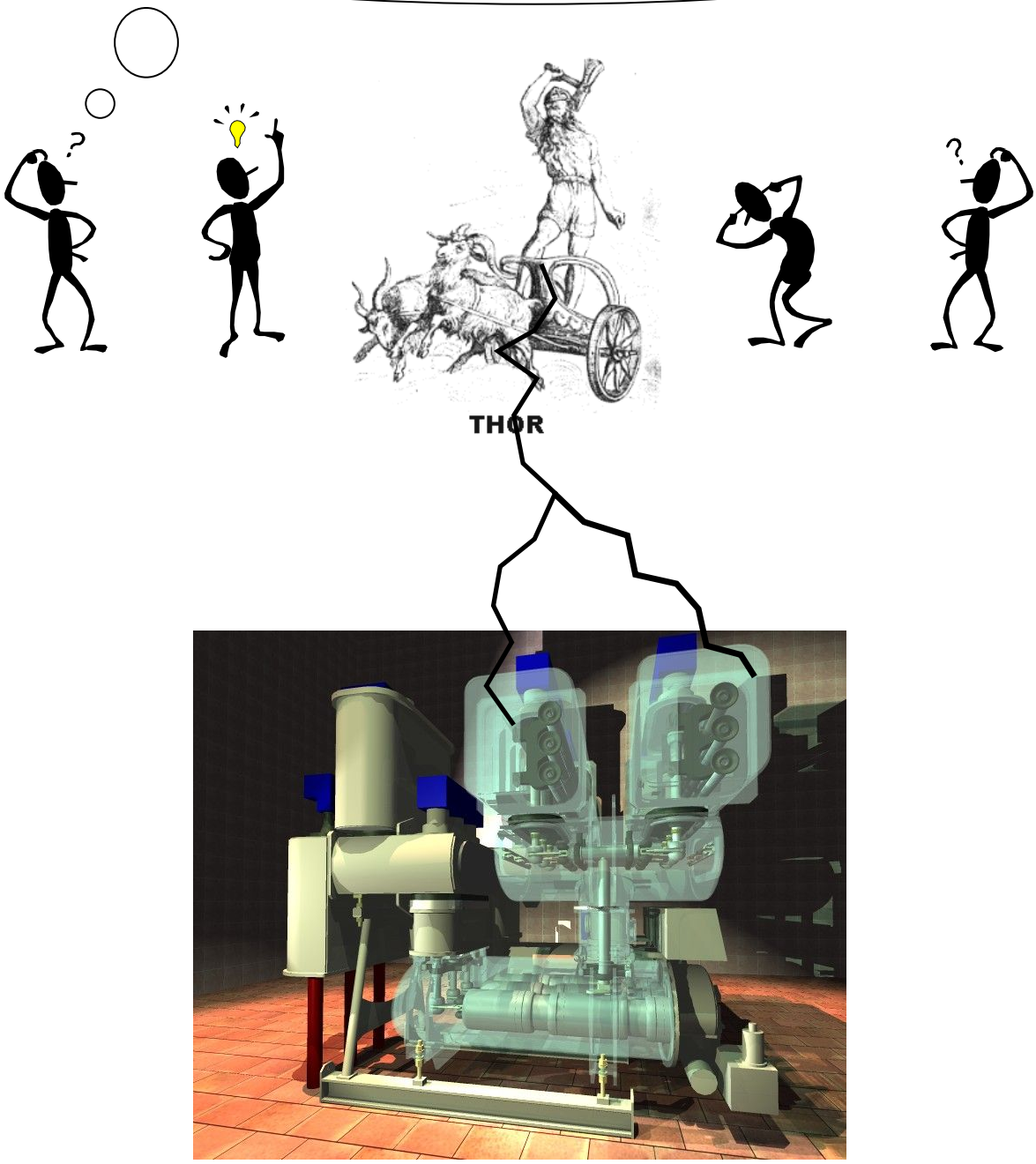
HIGH VOLTAGE CIRCUIT BREAKER TESTING WITH A FOCUS ON THREE PHASES IN ONE ENCLOSURE GAS INSULATED TYPE BREAKERS.



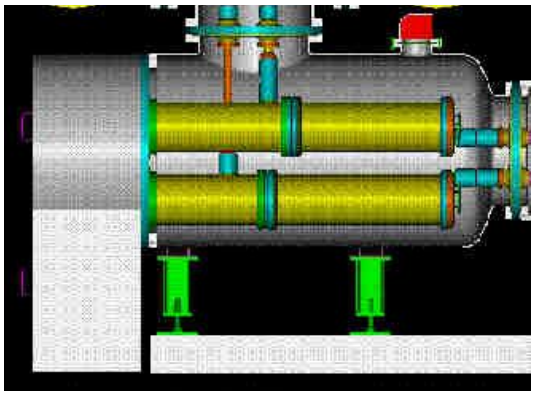
Adriaan Johannes Pieter de Lange.

Three Phases in one Enclosure Type Circuit Breakers (3PCBs);

Cover: VA-TECH ELIN HOLEC HIGH VOLTAGE BV, Amersfoort
Type: E-SEP, 245kV, 50kA

"Double busbar arrangement with cable connection"

Below: ENERGOINVEST, Sarajevo, Bosnia and Herzegovina
Type: MOP A3, 145kV, 31.5/40kA



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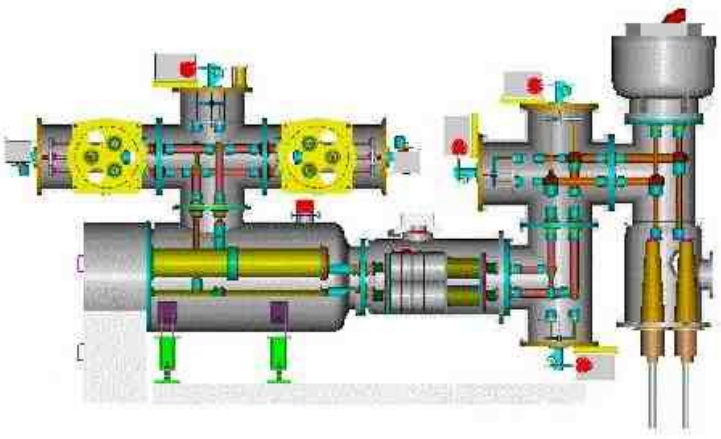

"Double busbar arrangement with cable connection"

HIGH VOLTAGE CIRCUIT BREAKER TESTING WITH A FOCUS ON THREE PHASES IN ONE ENCLOSURE GAS INSULATED TYPE BREAKERS.

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. ir. K.F. Wakker,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op maandag 13 november 2000 om 13:30 uur

door Adriaan Johannes Pieter DE LANGE

elektrotechnisch ingenieur
geboren te Alkmaar

Dit proefschrift is goedgekeurd door de promotor:
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ISBN: 90-9014004-2
NUGI: 832

Subject headings: HV circuit breakers, three-phase testing, switchgear

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In memory of both my grandfathers;

Dr. (h.c.) Johannes Hendrikus Kern, Nijmegen 1970 [1]
Dr.-Ing. Adriaan T.A.K. de Lange, Braunschweig 1931 [2]

The work described in this thesis was undertaken out of respect for both my grandfathers and my wish to do something similar. Financially, it was made possible by my wife Monique van Duijne, who was the sole breadprovider for three years.

Air, Land, Water and Electricity, are we Alchemists ?

You have to be when dealing with the electric Arc !

To; Monique, Anne and Pieter

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CONTENTS . Page:

1 Introduction..... 1
1.1 Electrical Energy, Transients and Circuit Breakers..... 1
1.2 Past and Present of Circuit Breakers and their Testing..... 3
1.3 Object of research..... 5
1.4 Outline of research..... 6
References..... 8
2 Circuit Breaker Development, Problems and Tools..... 11
2.1 (Test) Circuit Severity, historic and present status..... 11
2.2 Arc circuit interaction..... 12
2.3 Historical setting..... 12
2.4 A new quantification of thermal severity: Epa..... 14
2.5 Practical proof based on measurements..... 17
2.5.1 Analysis of the KEMA data..... 17
2.5.2 Statistical analysis of the KEMA-data..... 20
2.5.3 Computational aspects..... 23
2.6 The applicability of the post arc indicator: Epa..... 24
CASE A. SCHAVEMAKER ET AL.: TRV NETWORKS..... 24
CASE B. SHENG ET AL.: ULTRA HIGH VOLTAGE TEST CIRCUITS.. 26
CASE C. VAN DER SLUIS ET AL.: BTF TEST CIRCUITS..... 26
CASE D. BLAHOUS: VOLTAGE INJECTION TEST CIRCUIT 27
CASE E. ST-JEAN ET AL.: SYNTHETIC SLF TEST CIRCUITS..... 28
CASE F. URBANEK: SEVERITY ITRV AND SLF..... 29
CASE G. WEIL-DOBKE: INJECTION FREQUENCY AND TIMING..... 31
CASE H. CURRENT DEFORMATION IN A WEIL-DOBKE TEST CIRCUIT 32
CASE I. PERCENTAGE SLF SEVERITY FOR ABB AND GCB..... 33
CASE J. SCHNEIDER: PASSIVE PARALLEL ELEMENTS..... 36
2.7 Summary..... 37
References..... 38
3 Circuit Breaker Arc Models..... 45
3.1 Time-intervals in the interruption process of an electric arc..... 45
3.2 Arc models and their use..... 45
3.3 A historical Overview..... 48
3.4 A model for three-phase arc circuit analysis..... 50
3.5 Conclusion..... 54
References..... 56
4 The Network, Stresses on 3PCBs and the Standards..... 63
4.1 Introduction..... 63
4.2 History of Transient Recovery Voltage (TRV) Investigations..... 64
4.3 Common Network Topologies..... 66
4.4 Stresses in Overhead Line Type Networks..... 67
4.4.1 Meshed Overhead Line Type Networks (MOLTN)..... 68
4.4.1.1. Dielectric stresses..... 68
4.4.1.2. Thermal Stresses..... 70
4.4.1.3. Short Line Faults..... 72
4.4.1.4. Covering for Meshed Overhead Line Type Networks in a 3PTM..... 74
4.4.2 Radial Overhead Line Type Networks (ROLTN)..... 75
4.4.2.1. RRRVs in Radial Overhead Line Type Networks..... 76

4.4.2.2. Peak of Transient Recovery Voltage in ROLTN..... 77
4.4.2.3. Asymmetrical Short Circuit Currents in ROLTN..... 78
4.4.2.4. How to cope with ROLTN in a 3PTM..... 80
4.5 Stresses in Cable Type Networks (CTNs)..... 80
4.5.1 Substation Layout..... 81
4.5.2 System representation and substation equipment modelling..... 83
4.5.3 Analyses of TRVs in Cable Type Networks..... 85
4.5.3.1. Dielectric stresses in Cable Type Networks..... 85
4.5.3.2. Thermal stresses for 3PCBs in Cable Type Networks..... 86
4.6 Transient Recovery Voltages..... 88
4.6.1 The Benchmark system..... 88
4.6.2 Setting up the EMTP file with per unit elements..... 89
4.6.3 TRVs in Cable Type Networks..... 90
4.6.3.1. Five cases of TRVs in Cable Type Networks..... 90
4.6.3.2. Summary on TRVs in a Cable Type Network..... 95
4.6.4 TRVs in Radial Overhead Line Type Networks..... 96
4.6.4.1. Four cases of TRVs in a Radial Overhead Line Type Network..... 96
4.6.4.2. Summary on TRVs in a Radial Overhead Line Type Network..... 98
4.6.5 Which TRV is the most severe for the circuit breaker ?..... 99
4.6.6 Three-phase verification for the single-phase TRV computations..... 101
4.6.6.1. Setting up the three-phase network..... 101
4.6.6.2. Results of three-phase TRV analyses..... 102
4.6.6.2.1. Radial Overhead Line Type Networks..... 103
4.6.6.2.2. Pole to Clear Factors..... 106
4.6.6.2.3. Cable Type Networks..... 106
4.6.6.2.4. Radial Overhead Line Type Networks with an isolated neutral..... 108
4.6.7 Summary on single and three-phase calculations..... 110
4.7 Consequences for the Three-phase Test Method ?..... 110
4.7.1 Comparison between IEC 4-par values and the calculated results..... 111
4.7.2 Proposal for ‘adjusted’ parameters for Test Duty 3, 4 and 5..... 111
References..... 114
5 A Proposal for a Three-Phase Lumped Element Test Method (3PTM)..... 119
5.1 Introduction..... 119
5.2 Historical Overview..... 119
CASE A. BITSCH, RICHTER AND SCHRAMM, 1976..... 121
CASE B. DAMSTRA AND KEMPEN, 1980..... 121
CASE C. AZUMI ET AL., 1979..... 122
CASE D. MANGANARO, 1980..... 122
CASE E. BERNERYD, 1981..... 122
CASE F. NAKANISHI, 1982..... 123
CASE G. YAMAMOTO, 1984..... 124
CASE H. VAN DER LINDEN AND VAN DER SLUIS (KEMA), 1986..... 124
CASE I. FROEHLICH, 1987..... 125
CASE J. CIGRE WG 13.04 AND IEC SC 17A, 1989..... 125
CASE K. YAMASHITA ET AL., 1989..... 126
CASE L. NAKANISHI, 1990..... 127
CASE M. YOSHIZUMI AND SUGIYAMA, 1990..... 127
CASE N. VAN DER SLUIS ET AL., 1990..... 127
CASE O. IEC SC17 SUB 17A : IEC 61633, 1995..... 128
5.3 Requirements for a Three-phase Test Method..... 129

5.4 The ‘two-part’ test procedure (2PTP)..... 131
5.4.1 Dielectric tests..... 131
5.4.1.1. The basic operating principle for the dielectric test circuits..... 134
5.4.1.2. The symmetrical dielectric part test..... 136
5.4.1.3. The dielectric part test with asymmetrical current supply..... 141
5.4.2 The thermal part test..... 145
5.4.2.1. The operation of the SLF test circuit..... 146
5.4.3 Seamless TRV overlap dielectric and thermal part tests ?..... 150
5.5 Summary..... 151
References..... 152
6 Conclusion and Recommendations..... 157
6.1 Conclusion..... 157
6.2 Recommendations..... 158
6.2.1 Epa..... 158
6.2.2 Network stresses..... 159
6.2.3 Three-phase lumped element test method..... 160
List of Abbreviations and Symbols..... 161
APPENDIX I..... 163
APPENDIX II..... 180
Acknowledgements..... 185
Curriculum Vitae..... 186

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1 INTRODUCTION.

1.1 Electrical Energy, Transients and Circuit Breakers.

With the introduction of alternating current (AC) electrical energy as a versatile power source for every conceivable application by the end of the 19th Century, the problem of transporting and distributing this energy arose /a/.

In the case of changing the topology of a power system and protecting against (total) failure, the Circuit Breaker (CB) is an irreplaceable element.

Although it is commonly said that: "the circuit breaker opens the circuit", it is in fact the electric-arc (arc for short) formed inside the circuit breaker, which interrupts the circuit current.

How the arc is able to interrupt a (short-circuit) current is known through many years of practical experience and from the science of plasma physics e.g. /b,c,d,e,f,g,h,i,j,k/.

However, since many energy exchange processes play a role in the extinguishing process of the arc, we are still unable to predict, with a near to 100% probability, whether a (newly built) circuit breaker will interrupt a certain current in a specific circuit.

It is for this reason that circuit breakers are put to the test during the design and proving stages.

These tests are carried out in so called 'High Power Laboratories' /l/. High Power Laboratories test especially High-Voltage Circuit-Breakers in a separate test circuit, since in-grid-testing would jeopardize normal operations of the power system.

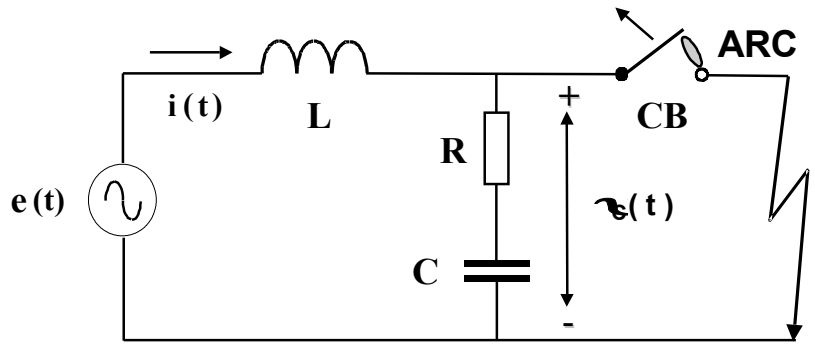
Test circuits try to simulate the most conceivable network or circuit conditions /m/.

This is quite difficult since the electrical phenomena which occur when a circuit is interrupted are rather complicated and depend on numerous network (and arc) conditions.

The most harsh conditions occur when a circuit breaker has to interrupt a short circuit current.
At first the breaker is subjected to a high current which heats it up considerably (or the arc for that matter) and by means of the accompanying Lorentz forces parts are put under great mechanical stress.
When the breaker interrupts the current (at a natural current zero) the subsequent Transient Recovery Voltage (TRV) subjects the breaker (or former arc channel) to a high dielectric stress.

Both phenomena, i.e. the high current and the high (transient) voltage, have to be withstood by the breaker and cannot be avoided in any way.

A simple representation of a short circuit interruption is given in figure 1.1.



e(t) = $E_m \cos\omega t$: e.m.f. of the supplying generators
L = synchronous reactance and leakage reactance of the transformers
C = capacitance of transformers, busbars, measuring equipment etc.
R = natural damping in the supply circuit
i(t) = resulting current through the CB before interruption
$\upsilon_c(t)$ = resulting voltage across the CB after interruption

Fig. 1.1 Short circuit interruption.

When the circuit breaker (or arc) interrupts the current i(t) we get when R is neglected:

$$L\frac{di}{dt} + \upsilon_c(t) = E_m \cos\omega t \quad \text{with} \quad i(t) = C\frac{d\upsilon_c}{dt}$$

or:

$$\frac{d^2\upsilon_c}{dt^2} + \frac{\upsilon_c}{LC} = \frac{E_m}{LC}\cos\omega t$$

Solving this second order differential equation gives:

$$\upsilon_c(t) = \left[\frac{\omega_0^2}{\omega_0^2 + \omega^2}\right] E_m\{\cos\omega t - \cos\omega_o t\} \qquad \text{with} \quad \omega_0^2 = \frac{1}{LC}$$

Usually $\omega_o >> \omega$ so, $\omega_o^2/(\omega_o^2+\omega^2) \approx 1$ and $\cos\omega t \approx 1$ during the time the transients play a role and we can approximate this to:

$$\upsilon_c(t) \approx E_m(1 - \cos\omega_o t).$$

This is the *Transient Recovery Voltage* (TRV for short).

However, in our example it is not a passing (transient) phenomenon since the resistance (R) has been neglected.

It has the characteristic '1-cos' form, which can be described as follows: the voltage wants to recover to the value it should have had at the moment of interruption if no short circuit had occurred, i.e. ~E_m, but it 'overshoots' this value, when damping is neglected, by a 100%.

1.2 Past and Present of Circuit Breakers and their Testing

Circuit breakers have been used since the beginning of electric energy distribution.

The first 'circuit breakers' were very simple open air, hand-operated 'knives' but soon they were put in some kind of containment and means were found to 'quench' the arc as well as possible.

Early circuit breakers used oil (or oil/water mixtures) to quench the arc but were of the plain break type. An example of this is given in /k/ where a circuit breaker for 200 – 300A at 40kV, made by a J.N. Kelman in 1901, is shown.

In the 1920s circuit breakers hindered further development of electric power systems and a worldwide search for their improvement was started /h/.

The oil plain break type was replaced by all kinds of oil circuit breakers with improved quenching by means of, for instance, an explosion pot, cross flow pump or a combination of these ideas /h/.

In as early as 1902 a circuit breaker design using compressed air was introduced /h/ because it had comparable quenching characteristics but was much less dangerous to operate than the types using oil.

This type of circuit breaker, like the oil type, was improved over and over again by such means as open air arcs, contained arcs, cross blow types, axially blown types, etc.

They were used together with oil circuit breakers depending on whichever type served the specific situation best.

Also as early as in the 1920s vacuum (thought to be applicable already by the end of the 19th century /n/) was investigated as a 'quenching' medium /o/, but in those days industrial processes were incapable of producing a bottle that could maintain a vacuum over an extended period of time and for a number of switching operations /p/.

The major problems were solved in the 1950s /p/ and since then this type of breaker has conquered the medium voltage range of applications.

In the 1950s SF6 was tested for its quenching properties /q/, as this gas had been known for its excellent dielectric properties since the 1940s.

It was found to be superior over oil and air and therefore SF6 has now virtually taken over the entire High Voltage range of applications and for the Extra High Voltage and Ultra High Voltage range it is the only medium in use.

Currently newly installed breakers are of the following types:

- low voltage range; (open) air breakers
- medium voltage range; vacuum or SF6 breakers
- high voltage range and above; SF6 breakers

Because SF6 has excellent insulating properties the latest trend of making designs more compact is only possible because of this gas.

Since all our combined knowledge of circuit breakers or the electric arc does not bring us a complete understanding of the interrupting process,

testing is indispensable in order to (re)assure whether or not a specific breaker will be able to withstand certain operating conditions.

The testing of circuit breakers is done in High Power Laboratories in so-called test circuits.

Several different test circuits have been in use since 1911 when AEG built the World's first High Power Laboratory (150MVA /nn/) in Kassel Germany.

Over the years, as our knowledge of the interrupting process progressed, ever-improving techniques have been developed to test the circuit breakers e.g. /l,r,s,t/.

These techniques were reflected in standards as, for instance, IEC and ANSI, be it with an understandable time lag.

Basically there are two types of test circuits to test circuit breakers. One is the *direct test circuit*, a circuit with only one power source to supply the necessary current before interruption and the necessary voltage after interruption and
the other is the *synthetic test circuit*, a circuit in which the necessary current before interruption and the voltage after interruption are put together by means of different power sources or through different paths of the test circuit.

The circuit of figure 1.1 is what we call a *direct test circuit* since there is only one power source which supplies the energy for both the short circuit current i(t) and the Transient Recovery Voltage $v_c(t)$.

In the beginning laboratories could keep pace with circuit-breaker developments /u,v/. However, at some point in time their 'direct-circuit-capability' became insufficient to test circuit breakers to their limits.

By then synthetic test circuits had been developed /w,x,y/ and over the years most testing stations were extended to accomodate for this type of testing /z,aa/.

In the beginning synthetic testing was the subject of extensive research to prove whether or not it was 'equivalent' to direct testing /bb,cc,dd,ee,ff,gg,oo,pp/.

Having found limits for the equivalence during the 1960s through theoretical and experimental research for air-circuit breakers mostly, from the beginning of the 1970s synthetic testing was generally accepted for all types of High-Voltage Circuit-Breakers (nowadays almost exclusively SF6).

As synthetic testing became the norm, many publications have gone into the subject in search for improved circuits /hh,ii,jj/ or their exact performance /y,kk,ll,mm/.

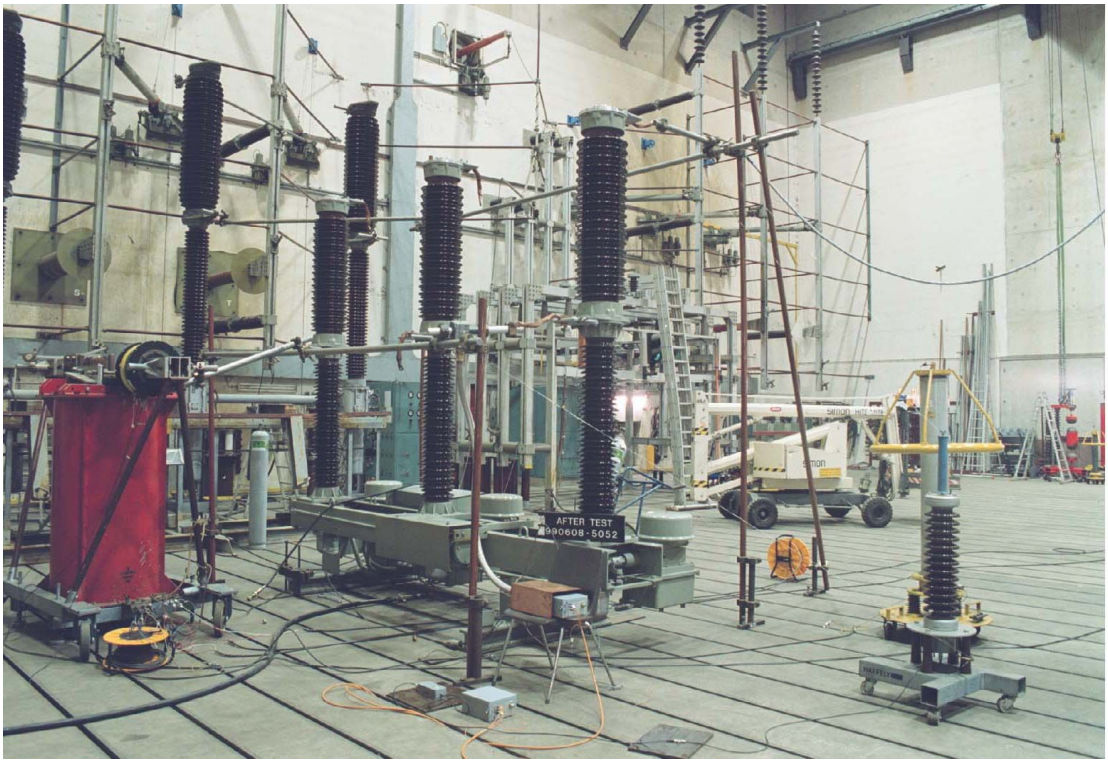


Fig. 1.2 Synthetic testing at KEMA.

1.3 Object of research

Developments in SF6 breakers make it clear that we have come a long way from the first SF6 breakers in the 1960s, which strongly resembled the double pressure air blast breaker.

This first generation was followed by a single pressure or puffer type breaker. In this type the opening action moves a kind of gas-pump of which the exhaust gas 'cools' the arc. The energy to move the puffer comes from the opening mechanism.

Because of its special gas properties, SF6 allows the use of the energy stored in the arc during the high current phase to help extinguish the arc at a natural current zero /1/. This phenomenon created the third generation of SF6 breakers, the so-called: self-pressurising breaker or self-blast breaker.

Another development is that the superior dielectric properties of SF6 make it quite easy to build all three phases together in one enclosure.
This so called Gas Insulated Switchgear (GIS for short) had been first built with air insulation by H.A. Hidde Nijland in the Netherlands in the 1950s, whereby the air-blast interrupters still had open exhausts.

Nowadays there are completely closed substations of the GIS type for voltages up to and including 550kV, like busses, voltage transformers, disconnectors etc. The circuit breakers themselves, however, were still separated per phase in the first designs.

Further requirements for diminishing the physical size of substations and circuit breakers in Megalopolis like Tokyo, Japan, led to the development of three-phases-in-one-(common)-enclosure type circuit breaker (3PCB for short).

With this type of breaker the concepts from the past were abandoned, as the usual distance between phases (or the usual earthed enclosures between phases) has disappeared and therefore the extinguishing processes in parallel arcs can influence each other through electro-magnetic coupling and hot exhaust gasses from neighbouring arcs.

The physical cross influences between phases inside the breaker itself, became a new aspect for circuit breaker testing.

In the past testing could be done single-phase since cross influences could be neglected; having to test only one (part) pole thus reduced the necessary testing power.

With 3PCBs, single-phase standard testing practices became more or less obsolete and insufficient to test for all possible failure modes.

The object of this research is to define a test method and synthetic test circuit(s) which tests the 3PCB for its failure modes, including cross influences between poles during interruption.

This research is conducted by examining the following main subjects: **circuit severity** or **arc-circuit-interaction**, **circuit breaker arc models**, **network characteristics** and **test circuit characteristics**.

These subjects are interrelated and require attention when considering a new test circuit or test method for testing High Voltage Circuit Breakers and 3PCBs in particular.

1.4 Outline of research.

The starting point is the subject of circuit severity or, as will be shown, arc-circuit interaction severity.

During the existence of the circuit breaker and the related test circuit research, arc-circuit interaction has played an important role.

This stemmed from the experience that:
Circuit breakers did not interrupt the same current in different networks
Circuit breakers also did not interrupt the same current in more or less identical test circuits

In Chapter 2 we will propose a new definition for the severity of the so-called thermal interruption interval around current zero and will make it plausible by means of results of practical experiments on SF6 breakers done by KEMA Arnhem, the Netherlands.

Thus having an instrument for calculating ‘thermal severity’ it will be used in the rest of this thesis.

As mentioned before, the phenomena which cause an arc to interrupt a current are not fully understood, let alone that the current limit could be predicted by some kind of model which includes every aspect of the processes involved.

In addition to this, although the network itself in which the circuit breaker is to operate is fully understood, network characteristics vary from one network to another but also over the years, since increased power consumption demands involve a continuous expansion of the networks.

The first problem, that we are unable to 'calculate' every aspect of the interruption process of an arc by means of a circuit breaker arc model, will be discussed in Chapter 3.

In this chapter we will investigate which type of circuit breaker model can be used best to model the behaviour of the SF6 arc in test circuit and network calculations.

The bottom line of this thesis is based on theoretical and numerical investigations and a literature study. Available results of practical experiments were used where applicable.

The next item, network characteristics, is the subject of Chapter 4.

Over the years network characteristics have been investigated quite extensively in order to define the stresses test circuits must exert on a test breaker /2/.

But power systems are not static and since test TRV characteristics were laid down in IEC in 1971, significant changes have taken place.

Such changes are, for instance, the use of high voltage cables on a much wider scale, the increase in voltage levels and the increase of power transported on a specific voltage level often leading to the splitting the network into a more radial structure as opposed to the usually meshed networks of today.

As will be analyzed in the chapter on network stresses, such changes involve different TRV characteristics, which are not reflected in current IEC standards.

The understanding acquired in Chapter 2, 3 and 4 will then be used to define a three-phase synthetic test method (3PTM), that accounts for the failure modes in a 3PCB to be tested. This is the subject of Chapter 5.

Chapter 6 contains the summary and conclusions of this work together with recommendations for further research.

The list of references at the end of each chapter is divided in two parts: references designated by a letter and references designated by a number.

The references with a number support a specific point, the references with a letter give the reader a general impression of the available sources and serve as a historical outline.

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bb) Zur Aequivalenz der synthetischen und direkten Pruefungen von Hochleistungsschaltern
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testing in view of the interaction between the arc and the circuit.
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2 CIRCUIT BREAKER DEVELOPMENT, PROBLEMS AND TOOLS.

2.1 (Test) Circuit Severity, historic and present status.

Circuit severity has been strongly related with circuit breaker research since people started testing circuit breakers.

The interest became less when IEC first defined the Short Line Fault (SLF) test and later the Initial Transient Recover Voltage (ITRV) duties.

At first it was more or less a mystery why a circuit breaker would interrupt a (short circuit) current in one part of the network but would not do so in another part of the same network and at the same current level.

It became apparent that the amplitude of the current to be interrupted and the natural frequency of the TRV played an important role, as becomes clear when reading for instance /a,b,hh/.

Test circuit severity and equivalence between test circuits have been subjected to much research as can be read in /c,d,e,f,g,h/.

The aim of a test circuit is to test a circuit breaker to its ratings in a reproducible way /1/.
The main topic for reproducibility is arc circuit interaction /2,3/.

Test standards (IEC) define circuit equivalence with a fixed rate of fall of current (di/dt) before current zero and a fixed rate of rise of voltage (dv/dt) after current zero, by means of two and four parameter TRV-envelopes /4,5,i,j/, with a maximum time delay.

This method, though criticized in some publications /5,6,7,67/ on the ground that this is not sufficient, has been the best option for many years as these requirements are easily ‘measurable’ for real tests in laboratories.

We will propose an additional criterion for numerical analyses: dissipated post-arc-Energy (***Epa***).

It will be made plausible that this additional criterion quantifies arc-circuit-interaction severity.

Such a criterion is a practical way to tackle the problem of arc-circuit-interaction, since all other approaches such as theoretical analyses and/or a large number of comparative tests are inconclusive, as can be read in /64/.
Or to speak with William Thomson (Lord Kelvin) 1824 - 1907:
“When you can measure what you are speaking about and express it in numbers, you know something about it.”

Using this criterion it can be said that a circuit breaker arc model resulting in the ‘same’ Epa in different test circuits, like a synthetic and a direct test circuit under standard ratings like IEC-60427 and IEC-60056 respectively, receives the same circuit stress.

2.2 Arc circuit interaction.

Arc circuit interaction has been looked at from many points of view /k,l/. Simplified (analytical) investigations /3,m,n,o,p,q,r,s/ led to interesting conclusions. Modern numerical analyses led to more detailed conclusions /8,g,t,u,v,w,x,y/.

In essence arc circuit interaction before current zero is the way in which di/dt of the arc current i_a and the arc voltage u_a result in a certain conductivity of the arc and to Electro-magnetic energy stored in circuit elements at the moment of interruption $i_a = 0$.
After current zero the dv/dt of the Transient Recovery Voltage (TRV) and post arc conductivity are dominant factors influencing arc circuit interaction. These effects are clearly analysed in /9/.

Since many parameters of the arc itself and parameters like the circuit characteristic impedance Z_C in relation with the arc resistance R_0 at the instant of interruption, play a role in arc circuit interaction, it is difficult to quantify arc-circuit-interaction by a single parameter.

The influence of the initial circuit conditions and circuit and arc parameters, is clearly shown by an analytical analysis of the Mayr-arc, operating in a simple RLC circuit using state space theory and Lyapunov's theory of stability /59/.

However, if we focus on the dissipated post arc Energy (Epa) we find some interesting things.

2.3 Historical setting

The thought that post arc phenomena might hold the key to solve the problem of circuit severity is not new since as early as in 1956 Cassie and Mason suggested that: "The power and total energy input (both post arc, AdL) are important factors in determining reignition and require careful study to relate them to circuit 'severity'" /10/.

In 1961 Rieder and Kuhn write:"…… Ergebnisse ueber die Wechselwirkung zwischen Schalter und Stromkreis vor und nach dem Nulldurchgang sowie ueber den Wiederzuendmechanismus. Sie (post-arc-current AdL) ist ein wichtiges diagnostisches Hilfsmittel bei der Beurteilung von Schaltern, Schaltbedingungen und Pruefkreisen." /jj/.

And in 1964 Cassie and Rieder (both members of the "Current Zero Club") sent a general appeal to interested parties in a publication in ETZ-A /11/ in which they stated that: "in order to tackle the difficult problem of 'circuit severity' interested parties are invited to do specialized measurements and acquire a whole list of data, including post arc phenomena."

In 1965 Cassie wrote: "Unfortunately, we do not yet know in detail how to relate 'severity' to circuit parameters in the case of energy (or thermal) breakdown." /12/.

In the same year (1965) Rieder stated: "Da verschiedene Kreise durch verschiedene Schalter in recht verschiedener Weise beeinflusst werden koennen, ist es kaum moeglich, die unbeeinflusste Spannungssteilheit durch ein einfaches und allgemeingueltiges Mass fuer ihre Beeinflussbarkeit zu ergaenzen." /13/.

And again in 1976 Rieder wrote: "Since the dependence of the breaking capacity of an unknown test breaker on these controlling circuit parameters (voltage, impedances, capacitances, resistances) or measured parameters (current and voltage waveforms) is not quantitatively known, the tolerances of the controlling parameters can only be determined empirically ……" /64/.

The History of 'circuit severity' goes back many years, as can be read in the excellent book by P. Hammarlund on Transient Recovery Voltages /14/.
In a special Chapter (G) Hammarlund discusses 'circuit severity' as it was investigated up to 1946.

As the story goes, it started with Kesselring who in 1931 doubted that simple breaking capacity defined in nominal power frequency MVA's should be retained.
In the following years, several definitions were tried, based upon theories of the time on how the switching arc manages to interrupt an AC current. Some theories are 'the race theory' /ee/ and 'the wedge theory' /ff,gg/.

Some definitions proposed were for instance:
Natural frequency of the circuit, recovery (surge) impedance or 'stiffness' of the circuit at the moment of interruption and Rated Rise of Recovery Voltage (RRRV) defined in several ways.

All the great names were involved. In alphabetical order,:
Biermanns, Boehne, Brown, Cassie, Flurscheim, Gosland, Julliard, Kesselring, Kopeliowitsch, Park, Peterson, Skeats, Slepian, Trencham and Van Sickle.

Hammarlund was in favor of the RRRV defined in a way Hochrainer would later (1957) use for his 4-parameter method.

However, the first peak values under 40% of power frequency recovery voltages were neglected.

This means that the Short-Line Fault (SLF) was not taken into account at that moment in time. And, as we will see further on, this happens to be the most severe type of fault where circuit severity is concerned.

The first publication about the Short-Line Fault (SLF) was by Pouard /z/ in 1958 and at the Cigre Conference that same year /aa/; the French (Mr. Renaud) discussed the phenomenon they had found to occur in their Networks and called: 'défaut kilometrique' during the discussions about the four-parameter method presented by Hochrainer in annexe II of report 151 /bb/. In fact it had been discussed before by the Germans /cc/, be it on the basis of natural frequencies (or /ii/ on the basis of distributed elements), as can be read in a paper by Hochrainer in 1959 /dd/.

In the 1930s and 1940s it was already noticed, however, that 'network severity' and 'test circuit severity' are not the same and Hammarlund deals with this problem in a full section of his Chapter G on 'circuit severity'.

With the formulation of the black box models /k,l/ and also influenced by the war, special attention was drawn to other aspects as well.

Then in 1956 Cassie referred to it again and in 1964 Cassie and Rieder launched their appeal to interested parties.

In 1968 the landmark paper on defining TRVs /15/ was published at a Cigre conference, written by specialists from all over the world.

They chose to 'close' the discussion by defining a delay time (as the Americans do) in combination with a well-defined RRRV (Hammarlund / Hochrainer method).

In 1971, after lengthy discussions and as an interim solution /63/, the 1968 proposals were incorporated in IEC-60056 (3rd edition), whereby the delay time is defined in a slightly different way, namely having the same tangent as the RRRV line.

Arc-circuit-interaction stayed on the agenda /63/ and over the years IEC-60056 was further improved at every revision, like by defining a separate Short Line Fault test and Initial TRV ratings.

The Current Zero Club started in 1960 by prof. D.Th.J. ter Horst played an important role in the development of ideas /kk/. This informal group was an ideal platform to discuss freely the many topics involved like: dynamic arc phenomena, arc electrode phenomena, reignition of open arcs, arcs in nozzle flow, arcs in SF6 gas, vacuum arcs, dynamic arc equations, current zero phenomena, problems of h.v. circuit breaker testing, short-line fault interruption, arc diagnostics and many more.
Under the supervision of the former (prof. ter Horst, prof. Hochrainer, prof. Rieder, prof. Damstra) and current (prof. Moeller) chairmans /ll/ the club met and meets on a regular basis and has contributed tremendously to all fields of circuit breaker research and their testing.

A steady number of papers was published and in 1988 Kertesz (visiting researcher at KEMA) mentioned in an internal report on arc-circuit-interaction: "despite of the great number of publications in this field (arc-circuit interaction, AdL), the problem cannot be considered to be solved." /60/.

2.4 A new quantification of thermal severity: Epa

To tackle the problem of arc-circuit-interaction we focus on the dissipated Energy during the post-arc regime (Epa).

Rieder and Kuhn also do this in their paper from 1961 /jj fig. 9/ but they do not further use this measure in their analysis.

In figure 2.1 a successful interruption is shown with its respective post arc current and post arc voltage. The calculated traces of post arc Power and post arc Energy are shown as well. Epa is defined as the post arc Energy (units Ws) up to the moment that the post arc current is lower than a certain low value.

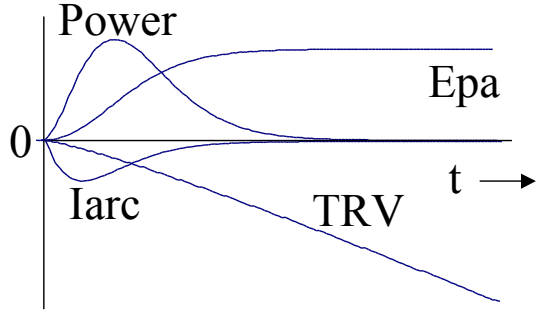


Fig. 2.1 Post arc voltage and current and calculated quantities

As limiting curves /16,17,18/ give a well-defined relation between circuit breaker capability and 'circuit severity', post arc energy (Epa) has a simple relation with di/dt and dv/dt.

When we put some Epa series of an Avdonin mathematical circuit breaker model /19,20/ in a graph, calculated in the EPRI/EMTP v2.1 Electromagnetic transients program, in a Weil-Dobke circuit (adapted in order to get independent di/dt and dv/dt rates) as described in /21/, we find figure 2.2:

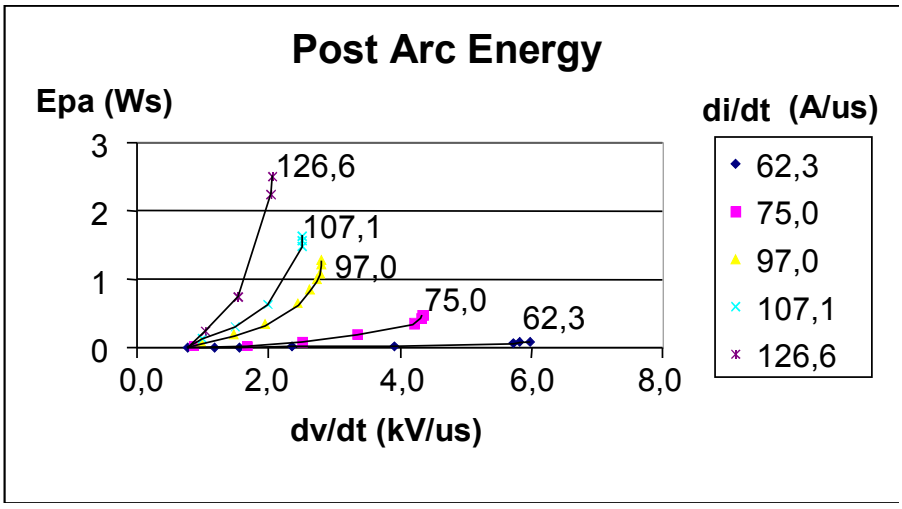


Fig. 2.2 Energy post arc (Epa).

Although rather unrealistic rates of di/dt were used, figure 2.2 shows that for a certain fixed di/dt up to the limit dv/dt, Epa increases along a simple curve.
This shows that Epa is directly linked to severity as di/dt and dv/dt are /71/.

Fig. 2.2 also shows that each curve has a maximum: Epa-max, after that point Epa goes to infinity because the circuit breaker model reignites. This maximum is related to the maximum interrupting power a circuit breaker can interrupt in this particular circuit for a certain di/dt:
the thermal limit /17/.

If we fit the five limiting dv/dt's of the di/dt curves, we obtain the empirical relation /22,23/:

$$\left(\frac{di_{\max}}{dt}\right)^{m}\left(\frac{dv_{\max}}{dt}\right) = Constant$$

with normally 1 <= m <= 1.5 and

$\frac{di}{dt}$ in A/µsec, $\frac{dv}{dt}$ in kV/µsec

with a very high degree of accuracy (σ = 0.018 and R^2 = 0.993).
For m and the value of the Constant we find: m = 1.521 and Constant = 3125.

The fact that the m found is outside the normal range found in practical circuit breakers is that: 1. It is an empirical relation with a certain spread and 2. We use an arc model, not a practical breaker.

The comparison shows that, although rather unrealistic rates of di/dt were used, the outcome of the numerical experiment is a realistic behaviour of a circuit breaker arc, despite the fact that a real SF6 arc is usually unable to interrupt currents with a di/dt > 40 A/μsec /70/.

More practical proof that post-arc phenomena (especially post-arc current) are a distinct 'signature' of a circuit breaker can be found in literature /17,24/.

As can be concluded from fig. 2.2, the di/dt (in fact what happens before current interruption) is of more influence for the thermal reignition than the dv/dt (in fact what happens after current interruption) but the dv/dt cannot be neglected.

When we take some data points from Figure 2.2 with fixed di/dt and some data points with fixed dv/dt and analyse their (relative) influence on Epa we find:

$$\frac{\Delta Epa}{\Delta di/dt} = 7.9 \qquad \text{and} \qquad \frac{\Delta Epa}{\Delta dv/dt} = 3.7$$

We see that in this case the relative influence of di/dt is about two times the relative influence of dv/dt.

Another support for Epa can be obtained if we repeat an experiment done by Birtwhistle et al. /68/.

In their paper the 50% interrupting probability /75/ of an Air-Blast-Breaker (ABB) is measured as a function of a parallel capacitance to the test breaker in a Weil-Dobke circuit.
A graph shows the relation for this ABB between the di/dt at which the interrupting probability is 50% and the value of the parallel capacitance.

We will now analyse, by means of a numerical experiment, the response of a Habedank circuit breaker model /61/ as a function of a parallel capacitance.
The Habedank arc model is to simulate a 245kV/63kA/50Hz ABB with a post arc current peak of about 3.5 amperes for about 35 microseconds when stressed with its nominal current and voltage ratings.

If we vary, for every point on the curve, the di/dt at a specific value of the parallel capacitance such that a certain fixed Epa (~0.27 Ws) is (re)produced in a Weil-Dobke circuit /21/, simulated in the transient program X-trans /25/, we get the curve of fig. 2.3:

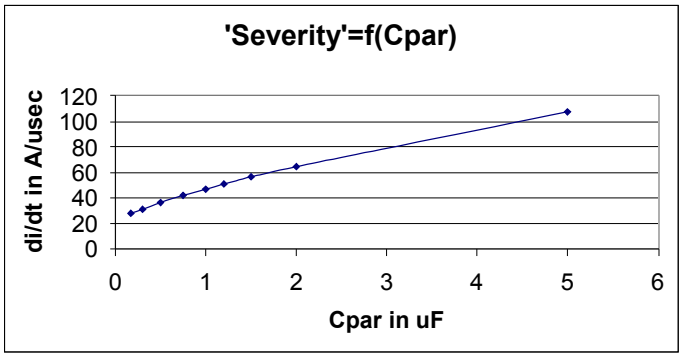


Fig. 2.3 'Severity' as a function of parallel capacitance.

This graph is very similar to the one Birtwhistle et al. found: an almost linear relation between 'severity' and the parallel capacitance for small values of Cpar and a lower linear rise for larger values of Cpar.

This shows again that Epa is a measure for 'severity', just as the 50% interrupting probability is.

2.5 Practical proof based on measurements.

A practical proof for Epa based on measurements can be obtained if we analyse current zero measurements done at KEMA in Arnhem, the Netherlands within the European Project SMT4-CT96-2121 /80/.

KEMA test engineers, with a newly installed current zero digital measuring system, are able to obtain very accurate measurement data of the current zero phenomena /73/. This was a further development of a 10 MHz system by Damstra and Kertesz which, by itself, was the result of a longstanding effort started at KEMA in the early 1950s by D.Th.J. ter Horst and G.A.W. Rutgers to acquire current-zero and post-arc measurements /82/.

From this data one can find the circuit breaker model parameters for the test breaker from the arc voltage and arc current before current zero in a short line fault duty (SLF).

The arc model is a modified Mayr model with three equations in series, whereby the different parameters, of each Mayr equation, are interrelated and the model as a whole is determined by three (3) free model parameters only. It was developed by V. Kertesz /80/.

If we use the model parameters from KEMA found for this phenomenological arc model based on real tests, we can draw several interesting conclusions if we calculate the post arc phenomena (Epa) in a simplified SLF-circuit (being a source with series inductance and resistance of 450 Ω in parallel to the arc).
Between tests, several 'severity' circumstances like ageing, which occurs naturally, or arcing-time and di/dt, which was deliberately done so, varied.

Trends in the calculated Epa values indicate that Epa is indeed a parameter which in just a relatively small test series, can tell something about the 'severity' of the arc-circuit-interaction (see example A in section 2.3) or about the condition of the circuit breaker after that particular test.

2.5.1Analysis of the KEMA data.

For a 123kV/31.5kA/60Hz Circuit Breaker for which the di/dt is varied but the arcing-time is kept constant, we find that Epa is rather small for the first few tests and increases slowly with the number of tests performed. Then a sudden jump of several orders of magnitude occurs and at the next test the Circuit Breaker Pole fails to interrupt (see Appendix I, table 1).
This end of life 'prediction' concurs with other measurements as well, as can be read in /76/.

If we put the 10 base logarithm of Epa in a graph in order to reduce its dynamic range for each pole, we acquire the figures 123.1, 123.2 and 123.3

as shown in Appendix I. *From these figures a 'steady' increase of Epa can be recognised*.

A higher current amplitude and thus a higher di/dt is more severe and ages the pole at a higher rate since Epa values increase and the number of successful tests per pole decrease.

So, we may conclude so far that, Epa is an indicator for the condition of the circuit breaker (pole).

As the number of tests increases, the ablation of the nozzle increases and the gas of the breaker (pole) is more and more contaminated, so after about 10 tests this ageing hinders the interruption processes to such an extent that the breaker cannot interrupt the current anymore.[1]

Fig. 2.4 Synthetic SLF test of 123kV Circuit Breaker at KEMA.

For a 72.5kV/31.5kA/60Hz puffer Circuit Breaker for which the current zero phenomena were measured at several consecutive current zero crossings per test (segment 2, 3 and 4), we find a similar trend (see Appendix I, table 2 column 'Epa nWs; KEMA').

During the first few tests each breaker pole is capable of interrupting (I) the current at the second current zero crossing (segment 3), when the arcing-time has been long enough to build up nozzle-clogging sufficiently, then Epa jumps several orders of magnitude and the breaker pole is hardly capable of interrupting the current at the 3rd current zero crossing (segment 4) and after that the breaker pole starts to reignite (R) in the next tests.

This is in particular visible for the long test series on pole C with a reduced di/dt stress.
Since the number of interrupted tests rises with a decreasing di/dt, like for pole A 14 A/µsec and 5 interruptions, for pole B 12 A/µsec and 6 interruptions and for pole C 9 A/µsec and 13 interruptions, it is obvious

[1] In our opinion, Epa can be used to define a circuit breaker (type related) maintenance schedule.
Based on post-arc-currents such an idea has been investigated in the past by Rieder and Kuhn /jj/.

that di/dt (or peak-current for that matter) is important where severity is concerned.

If we repeat this analysis with the measured voltage and current traces for the 72,5kV/60Hz SF6 circuit breaker fitted onto another modified Mayr model developed by Schavemaker at Delft University and this time insert this model into the 'real' SLF-test-circuit (with as many details such as stray-capacitances to give a most realistic circuit) and again calculate the Epa-values, again we find the Epa-series in the column 'Epa uWs; TUD'.

Although the 'jump' in Epa towards the end of the lifecycle of the circuit breaker pole is less pronounced as compared to the Epa-series found by means of the Kertesz model in the simplified SLF circuit, the same trend can be recognised (see Appendix I table 2).

If we take the 10 base logarithm of each Epa, in order to reduce its dynamic range, and put these values in a graph, *the general trend, i.e. Epa increases from test to test and jumps towards the end of the lifecycle, is clearly visible* (see in Appendix I figure 72.1, 72.2 & 72.3).

For a 145kV/31.5kA/60Hz puffer Breaker the current zero phenomena were measured at several consecutive current zero crossings per test (segment 2, 3 and 4) as well, see in Appendix I, table 3 and figure 145.1 and 145.2.

Epa values in table 3 were found by means of the new-KEMA model (Kertesz-model) put in the simplified SLF-circuit as explained earlier. The figures 145.1 and 145.2 were made by taking the base 10 logaritm of these Epa values.

For the first few tests on pole C (in a Direct SLF-Circuit) this breaker is capable of interrupting the current in the second current zero crossing (segment 2). Then Epa increases sharply and the breaker is hardly capable of interrupting the current in this current zero crossing. At the next test the breaker needs a much longer arc-time to build up its cooling power, 16 msec instead of 12 msec, and Epa drops again.
Then a search for its minimum arc-time, starting from 16msec to 9msec, produces erratic Epa-levels caused by the stochastic behaviour of the arc.

Although the behaviour is erratic the drop in Epa-levels on both poles around an arc-time of 13 - 14 msec could very well be an indication of the fact that the breaker has a superiour interrupting capability around this arc time.

It is the arc itself which causes the stochastic behaviour of a circuit breaker and not for instance its open/close mechanism or the contacts, as can be read in a paper by Hochrainer /74/.

When ageing this breaker pole around an arcing-time of 15.5 msec, again one recognises the familiar increase in Epa-values.
It must be mentioned that this is a very good breaker that could probably handle some more tests which were not done since the test-shift had come to an end.

The second pole (B) of this 145kV breaker is tested in a Synthetic SLF-Circuit.
When we observe the differences between the Test Series of this pole and the last, we find that the Synthetic Test Series is much more regular, because the spread in Epa is much smaller.
The reason for this is that a Direct Test Circuit is usually more severe than a Synthetic Test Circuit, which is caused by the fact that the

'thermal severity' of a direct test is usually higher than the 'thermal severity' of a synthetic test (as will be discussed later) and this in itself could be the cause of the larger spread in Epa-values.

The ageing process on this pole, towards the end of the lifecycle, is not clear since the increase in Epa-values is better explained by the steady reduction of the arcing-time.
Also this pole of the breaker could most probably have handled some more tests if the test-shift had not come to an end due to which no more tests could be done.

Because the tests on both poles had to be stopped before a pole was tested until destruction, this could be the explanation why the expected sudden increase in Epa does not show-up.

Another way of using the KEMA-datasets is by correlating the Epa-series to another 'severity or stress'-parameter, such as the ratio S/SL.

This parameter denotes the ratio of the actual di/dt: S of a test over the maximum achievable di/dt: SL, the derived CB-model is capable of interrupting in the simplified circuit, consisting of a voltage source with current limiting inductance (5.2 mH) and a 450 Ω resistance in parallel to the CB-model (to account for the characteristic impedance of the transmission line).

An interpretation of the S/SL ratio is that if this parameter S/SL is nearly one or even greater than one it indicates that the test was rather 'severe' and if S/SL is considerably smaller than one it indicates that the test was not so 'severe'.
Seen from the breaker perspective $S/SL < 1$ indicates that the performance of the breaker in that particular test was relatively good and $S/SL \approx 1$ indicates that the performance of the breaker was marginal and that it is reaching the end of its life.

If we put both, Log(Epa) and S/SL per Circuit Breaker in a graph, we get the results shown in Appendix I figure 123.S, 72.S and 145.S.

From these graphs we see that the correlation between Log(Epa) and S/SL is very good and we conclude that Epa can be used as a measure for the 'stress' or 'severity' a circuit breaker is subjected to.

2.5.2Statistical analysis of the KEMA-data.

Using the same KEMA-data from the SLF-tests on the 72.5kV, 123kV and 145kV breakers, we have investigated three indicators for 'severity' or Circuit Breaker ageing, i.e. the value of the arc resistance at current zero: R0, the ratio: S/SL and the value of Epa.
With the help of several statistical tests (such as ANOVA, regression analysis and non-parametric tests) we investigated whether these indicators do tell something about the condition the breaker under test is in and which indicator is the most useful.

In the first comparison /77/ we investigate the usefulness of the ratio S/SL and the Epa value and compare them with each other.
The analyses are based on the results of KEMA calculations with the Kertesz-model in a dedicated program to find the ratio S/SL and on calculations with the same Kertesz-model and parameters done with the X-trans computer program.

In this analysis we look for instance for the correlation between either the Epa value or the ratio S/SL and the number of times the breaker *in reality* successfully switched-off or an approximation of the cumulative amount of energy absorbed during the high current phase for every consecutive *successful* test.

The absorbed arc-energy is calculated with:

$$E_n \cong \sum_n \int i^2(t).dt \qquad n: \text{successful test number}$$

In the second analysis /78/ we investigate the relative merit of the value of R0, the arc resistance at interruption, and the Epa value by comparing them with each other.

Both, parameters (R0 & Epa) and analysis in /78/ are based on the results of calculations done by Schavemaker /79/ with the Habedank-model /61/ in Matlab with the same KEMA-dataset taken as a starting point.

Schavemaker generated this data by fitting the pre current zero voltage and current traces to three arc-models: Kertesz, Habedank and Schavemaker for each test.
He then used these arc-models (and parameters) to find each indicator (S/SL, Epa and R0) for a range of digital SLF-tests (80% - 97%) in the full circuit for each real test result.
This data was then made relative by dividing each single result by its maximum for that real test (see also section 2.6 Case I).

We then traced the correlation between the Epa value or the value of R0 and the number of times the breaker *in reality* successfully switched-off.

From both analyses we can conclude, as expected, that the Epa value is, with a rather high degree of determination (r^2), interrelated to the ratio S/SL or the value of R0.

In fact each pair of indicators (Epa;S/SL, Epa;R0) could be interpreted as both sides of the same coin.

From the first analysis we can conclude that the ratio S/SL is better suited than the Epa value to give information about Circuit Breaker ageing.
From the second analysis we find that the Epa value is a better indicator than the value of R0 to inform us about Circuit Breaker ageing during short circuit tests.

To display some of the results we will table the F-statistic for a linear regression between Epa (or R0 or S/SL) and the cumulative absorbed energy in the arc: E_n, based on the data generated by Schavemaker /79/.

Strictly speaking a linear regression ($y_i = \beta_0 + \beta_1.x_i + \varepsilon_i$) is only applicable if:
$\varepsilon_i \sim N(0,\sigma)$, $Cov(\varepsilon_i, \varepsilon_i) = 0$ and x_i = non-stochastic and non-correlated.
For the analysis it is assumed that this constraint is true.

An ANOVA-analysis on the regression line tells us to what degree the variance in Epa, R0 or S/SL is explained by the simple linear relation. This is expressed by the F-statistic. If the F-statistic exceeds a certain critical value F* there is a linear relation between the indicator and the calculated accumulated arc energy: E_n.

F-Statistic	Epa	R0	S/SL
72.5kV; 10 obs.	**5.61**	**0.10**	**9.30**
123 kV; 21 obs.	**8.84**	**10.84**	**27.17**
145 kV; 41 obs.	**6.10**	**2.65**	**1.05**

TABLE 2.1A

IT IS OBVIOUS THAT WE CAN ONLY COMPARE F-STATISTIC VALUES FOR THE SAME SET OF DATA (OBSERVATIONS = OBS.) FROM ONE TYPE OF BREAKER AND NOT BETWEEN BREAKERS.

FROM THIS TABLE WE CAN CONCLUDE THAT FOR THE 72.5 KV BREAKER THE S/SL RATIO IS THE BEST INDICATOR (HIGHEST F-STATISTIC), FOR THE 123 KV BREAKER THE S/SL RATIO IS ALSO THE BETTER INDICATOR AND FOR THE 145 KV BREAKER EPA IS BEST SUITED.

IF AN 1% LEVEL OF SIGNIFICANCE IS ASSUMED THE CRITICAL F* VALUES ARE:
F*(72.5KV) = F(1,8,0.01) = 11.26,
F*(123KV) = F(1,19,0.01) = 8.18 AND
F*(145KV) = F(1,39,0.01) = 7.31.

SO, AT THIS LEVEL OF SIGNIFICANCE WE HAVE TO CONCLUDE THAT ONLY FOR THE 123KV BREAKER THERE IS A LINEAR RELATION BETWEEN THE THREE INDICATORS AND THE CALCULATED CUMULATIVE ARC ENERGY E_n.
For the other breakers we have to ease our requirement to a higher level of significance of 2% before we can accept a linear relation between at least one of the indicators and the calculated cumulative arc energy E_n.

If we table the corresponding critical F* values, we get:

Critical-F*	Epa	R0	S/SL
72.5kV; 10 obs.	**0.0454**	**0.7652**	**0.0158**
123 kV; 21 obs.	**0.0078**	**0.0038**	**4.96E-05**
145 kV; 41 obs.	**0.0180**	**0.1116**	**0.3126**

TABLE 2.1B

THE CRITICAL F* VALUES ARE A RELATIVE MEASURE AND CAN THEREFORE BE USED FOR COMPARISON BETWEEN BREAKERS.

SO, EPA HAS RELATIVELY LOW CRITICAL F* VALUES FOR EACH OF THE THREE BREAKERS, WHEREAS BOTH R0 AND S/SL ARE SOMETIMES NOT USEFUL AT ALL.

On the basis of all the statistical tests of /77/ and /78/ comparing S/SL, Epa and R0 with each other and other parameters like E_n or the number of times the breaker has successfully interrupted the current, we can draw the conclusions that:

- S/SL is best suited to indicate CB-ageing if very accurate (digital) current zero measuring systems and sophisticated numerical analysis tools are available.
- Epa is best suited to quantify the arc-circuit-interaction (please see below in section 2.6 Case A) and can be used to compare (test) circuits as well.
- R0 is the least applicable of the three indicators.

2.5.3Computational aspects

In the last section we applied linear and nonlinear differential and algebraic equations to model the circuit and the arc.

Although linear differential and algebraic equations are a linear approximation of the Maxwell equations to describe electro-magnetic phenomena in electric circuits, they are widely used in combination with numerical solution techniques in computer programs for the calculation of these phenomena in electric circuits.

The fact that (rather simple) nonlinear differential equations describe the phenomenological (or black box) behaviour of the electric arc is less well known.

But it is a well-established practice because many years of worldwide research have proven this fact. More will be discussed in the chapter on circuit breaker modeling (Chapter 3).

For all analyses, the results of which will be shown later on, two transient analysis tools: 1) EMTP and 2) X-trans, were used.

Both tools are capable of simulating the electric arc and electric transient phenomena in a (test) circuit /20,25/.

To show that both programs are correct, we will - with both tools - do a simulation of a direct test on a circuit breaker simulated by an Avdonin circuit breaker model.

The circuit breaker model parameters were taken from St-Jean /26/ in which case P_0 was reduced to produce a rather late thermal failure:

$$\tau_0 = 6,0\mu sec \ , \ \alpha = 0,2 \ , \ P_0 = 30MW \text{ and } \beta = 0,50.$$

If we put both current traces around current zero in a graph we get:

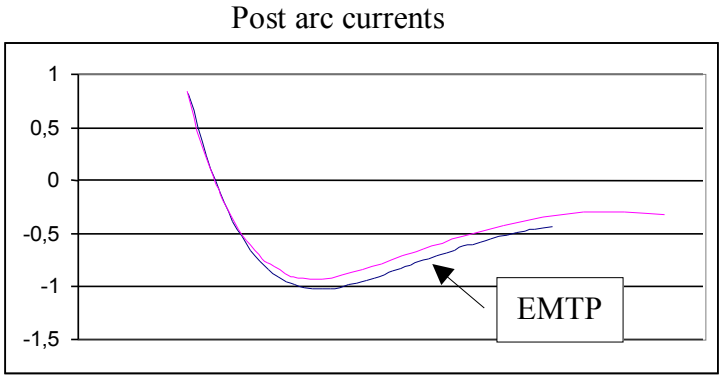


Fig. 2.5 Effect of numeric errors on calculations

Since the two curves are almost identical, we may conclude that both programs correctly integrate the same differential and algebraic equations, be it that the EMTP (lowest curve) with its trapezoidal rule and fixed time step, as opposed to the BDF-method (Gear-routines) /27/ with its variable time step used in X-trans, produces a slightly higher post arc current peak.

Secondly, we may conclude that one cannot compare Epa values of two identical breaker models operating in two identical circuits but calculated with two different numerical solution techniques, in this respect: EPRI/EMTP and X-trans, since the post arc currents (and thus the TRV as well) differ slightly; and therefore Epa values will not be identical.

Epa comparison has to be made within the same numerical technique and program.

A comparison between Epa and other indicators, like R0 or S/SL, can be made with different tools if each indicator is found by using one and the same tool for all data samples involved. However, to overcome a possible systematic difference between one tool and the next it is preferable that all calculations are done in one and the same tool.

2.6 The applicability of the post arc indicator: Epa.

To show the use of the post arc Energy indicator (Epa), we will discuss several well-known problems in circuit breaker testing as discussed in literature in Case studies A to J. However, this time we will analyse them by means of Epa.

Case A. Schavemaker et al.: TRV networks

As a first example we will compare eight direct circuits as published by Schavemaker and van der Sluis /28/ (circuits and parameters are given in Appendix I Case A).

We will evaluate the order of severity for those eight circuits using EPRI/EMTP v2.1 and a Kopplin circuit breaker model and repeat the exercise using X-trans with a KEMA circuit breaker model /29/ which is, in the post-arc region, a different model as compared to Mayr derivatives /30/, such as the Kopplin model.

Two different numerical techniques and two different arc models are used.

A higher Epa indicates a more severe interaction between the arc and the test circuit.

Apart from Epa, another indicator for interruption severity: the arc resistance at interruption R_0 (units Ω) is tabled.

The R_0 indicator is a measure for severity until the instant of interruption, which includes current deformation and a higher R_0 means a less severe arc circuit interaction.

As noted by Schavemaker and van der Sluis, all direct circuits produce an almost equal inherent TRV, but the circuit topology and the characteristic impedance at interruption are different.

The TRVxR circuits have a lower surge impedance than the TRVxC circuits (Z_R=150Ω < Z_C=225.2Ω). Furthermore, the TRVxC circuits all have a time delay capacitance C_d directly parallel to the breaker whereas the TRVxR circuits lack this capacitance.

	TRV1C	TRV2C	TRV3C	TRV4C	TRV1R	TRV2R	TRV3R	TRV4R
EMTP Epa	**0.021028**	**0.021492**	**0.021361**	**0.020885**	**0.029702**	**0.030819**	**0.031028**	**0.029203**

Epa order	E_{Epa}-II	E_{Epa}-IV	E_{Epa}-III	E_{Epa}-I	E_{Epa}-VI	E_{Epa}-VII	E_{Epa}-VIII	E_{Epa}-V
EMTP R_0	**1103**	**1019**	**1048**	**1121**	**727.7**	**699.5**	**733.3**	**745.8**
R_0 order	E_{R0}-II	E_{R0}-IV	E_{R0}-III	E_{R0}-I	E_{R0}-VII	E_{R0}-VIII	E_{R0}-VI	E_{R0}-V
X-trans Epa	**0.103226**	**0.101111**	**0.101495**	**0.102957**	**0.104620**	**0.103151**	**0.101886**	**0.104372**
Epa order	X_{Epa}-VI	X_{Epa}-I	X_{Epa}-II	X_{Epa}-IV	X_{Epa}-VIII	X_{Epa}-V	X_{Epa}-III	X_{Epa}-VII
X-trans R_0	**228.5**	**229.2**	**217.5**	**220.8**	**184.7**	**183.7**	**185.0**	**186.6**
R_0 order	X_{R0}-II	X_{R0}-I	X_{R0}-IV	X_{R0}-III	X_{R0}-VII	X_{R0}-VIII	X_{R0}-VI	X_{R0}-V

Table 2.2

From table 2.2 it can be concluded that TRVxR is always more severe than its 'delayed' counterpart TRVxC, no matter if we compare the post arc energies Epa or the resistance R_0 at current zero.

This is explained by the fact that test circuit severity is to a great extent influenced by the capacitance directly parallel to the test breaker /24,31,32/.

The larger this capacitance, the higher the limiting curve will lie above the theoretical straight line that can be found by analytical investigation for a 'Mayr' arc model interrupting a fixed di/dt and fixed dv/dt /33/, or the longer the time constant of the arc τ can be /34/, the easier the test breaker can interrupt a current and the lower its Epa will be.

From this analysis we can see that the order of severity (I=lowest, VIII=highest) is not the same for the EMTP and X-trans Epa analyses or for the EMTP and X-trans R_0 analyses.

This is caused by the fact that we used two different arc-models and the fact that the different numerical solution techniques give slightly different solutions, which can be noticed immediately from the TRVs even though inherent TRVs show an extreme similarity between different circuits.

This supports the fact that through a macroscopic analysis with black box circuit breaker models like Mayr and KEMA models and circuit modeling with Kirchhoff's laws, it is not possible to disentangle arc circuit interaction and define 'a most severe circuit' neglecting the arc (model); we have to speak about *arc circuit severity*.

This conclusion is not new and was already made by Biermanns /69/, on the basis of a very simple qualitative analysis of an arc in a simple direct circuit with parallel damping.

The analysis also makes it clear that we cannot use a simple Epa comparison with real test data as a measure for arc-circuit severity, since circuit breakers also show a so-called stochastic behaviour /35,36/: two tests under identical conditions will most probably give different Epa results.

Only a statistical comparison of Epas over a large number of tests gives more precise results.

The Epa method includes pre-zero *and* post-arc effects and clearly discriminates between arc-circuit combinations.

Other methods which include both pre-zero and post-arc effects are varying a circuit breaker parameter like the filling pressure and detect the lowest pressure at which the arc model still interrupts /37/. This method also discriminates, but by changing an arc model parameter, arc characteristics and therefore arc circuit interaction changes too.

Epa is more effective for the complete time span of arc circuit interaction (or thermal severity /38/) and *can be determined without influencing the arc or circuit characteristics.*

Case B. Sheng et al.: Ultra High Voltage test circuits

As a second example we will compare four Ultra-High-Voltage (UHV) test circuits, being the reference direct circuit, the EPIC circuit /39/, the Hitachi circuit /40,41/ and a standard voltage injection circuit for their inherent TRV responses (circuits are given in Appendix I case B).

When we compare the first 10 μsec of the inherent TRV responses we find that they are almost equivalent.
This short time interval is critical for an UHV SF6 circuit breaker with respect to the so-called: thermal reignition.

Arc circuit interaction, however, disrupts the similarity of the initial TRV's. For instance: the Voltage Injection scheme has a steeper TRV during post arc conductivity when an arc model simulates the circuit breaker behaviour concerning arc-circuit-interaction.

Sheng /39/ uses the arc resistance at interruption (R_0) to compare arc circuit severity which, as explained, can be used as a measure but is less sensitive because it includes arc-circuit-interaction up to current interruption (i_a = 0) but does not account for post arc effects.

Comparing the four circuits with respect to post arc energies (Epa) and the value of the arc resistance at interruption (R_0) for a 765kV/63kA/50Hz SF6 circuit breaker modeled by a Kopplin model with $K_t = 3.5^E-6$ and $K_p = 7.0^E+6$ [V_{con} = 2400 V] gives:

	Direct	EPIC	Hitachi	Volt. Inj.
Epa (Ws)	**2.5577^E-5**	**5.8838^E-6**	**1.2511^E-5**	**3.1374^E-5**
R_0 method (Ω)	**38.4 k**	**123.9 k**	**96.2 k**	**40.4 k**

Table 2.3

From table 2.3 we see that the arc circuit severity in decreasing order is: Voltage Injection, Direct, Hitachi and EPIC producing the least severe interaction.
This is *not* the same conclusion Sheng finds and also an order different from the one we find when using the R_0 method.

The wave forms indicate that the voltage injection scheme produces a slightly deformed TRV (steep rise directly after interruption) which influences the thermal stress to a great extent.

It would be premature, however, to conclude that one circuit is more 'severe' than another. In that case one would have to compare Epa values for a larger number of arc models and breaker ratings to make such a statement based on averages.

Case C.Van der Sluis et al.: BTF test circuits

As another example of the use of Epa we will compare the test circuits compared by vdSluis/Rutgers in /37/ (circuits are given in Appendix I case C).

This paper compares the Direct, Weil-Dobke and Hitachi test circuits for a IEC-60056 Test Duty 4 test on a 245kV/40kA (60Hz) SF6 circuit breaker.

In order to find which of the two test circuits, Weil-Dobke or Hitachi, is the best equivalent of the direct circuit, in /37/, the P-method (Pressure at t=0) on a circuit breaker modeled by the KEMA model is used.
As explained before, this method may be used as an indicator but by changing the gas pressure the arc-characteristics and subsequently the arc-circuit-interaction also change.

When we analyse the circuits in EPRI/EMTP v3.0 with the new implementation of the Urbanek model /42,43/ artificially set to simulate an SF6 breaker, we get the following results:

	Direct circuit	Weil – Dobke	Hitachi circuit
Epa (Ws)	**0.00924022**	**0.00792008**	**0.14053429**

Table 2.4

As will be shown later, the moment of triggering for the Weil circuit does influence equivalence. So it is set to give optimum equivalence.

Table 2.4 leads to the conclusion that the Hitachi circuit is more severe in the thermal region. This is caused by the fact that it has no lumped delay capacitance.

If we add this capacitance, accepting the fact that the IEC delay time t_d is increased (3 μsec in stead of 2 μsec), we get Epa = **0,01075217** Ws.
This is only marginally higher than the arc-circuit-severity of the direct circuit.

Beside the clear influence of a parallel capacitance this result also indicates that the IEC delay time concept (t_d) is not the solution to define thermal stress.

Therefore it can be concluded that the original Weil-Dobke circuit is the best 'equivalent' circuit to test SF6 circuit breakers as compared to the direct circuit.

If we now take the same circuits but insert an Air Blast Breaker modeled by a Kopplin model with a relatively long time constant (causing a high and long post-arc current) we get a totally different picture:

	Direct	Weil - Dobke	Hitachi
Epa (Ws)	**70.9**	**24.1**	**19.5**

Table 2.5

Now the direct circuit is the most severe. This is caused by the fact that the TRV from the synthetic circuits is deformed more by the post arc current than the direct circuit TRV.

The Hitachi circuit is now even less severe than the Weil-Dobke circuit.

We conclude that one has to compare (test) circuits with average Epas found from a large number of analyses with different arc models in order to be able to state which circuit has the best equivalence or is more severe.

Case D.Blahous: Voltage injection test circuit

A next case which shows the abilities of a tool like Epa is when we compare the severity of one of the voltage injection circuits of Blahous (Blahous#4) /44/ with the severity of the direct circuit using X-Trans and a circuit breaker modeled by the KEMA arc model (Rutgers model). Circuits and arc parameters are given in Appendix I case D.

In his paper Blahous shows that a resistance R_p parallel to the Auxiliary Breaker (AB) in a simplified voltage injection circuit does influence the 'severity' for the Test Breaker (TB).

We find the same thing with the use of Epa and get:

Direct circuit ***Epa* = 0.06226 Ws**	Blahous#4,Rp=450Ω ***Epa* = 0.08184 Ws**	Blahous#4,Rp=350Ω ***Epa* = 0.07843 Ws**	Blahous#4,Rp=150Ω ***Epa* = 0.07006 Ws**
	Blahous#4, Rp=50Ω ***Epa* = 0.06190 Ws**	Blahous#4, Rp=60Ω ***Epa* = 0.06018 Ws**	Blahous#4,Rp=500Ω ***Epa* = 0.07923 Ws**

Table 2.6

The voltage injection circuits have the same circuit topology and circuit elements and the test breaker and auxiliary breaker models have identical parameters too, except that the resistance R_p varies.

Table 2.6 shows that R_p influences arc circuit severity. Furthermore it becomes clear which circuit (R_p = 50 Ω) is best equivalent to the direct test circuit.

We find a different value for R_p from Blahous, which can be explained as following:

- Blahous based his conclusions on the interpretation of voltage and current traces only.
- The timing of the spark gap is different from Blahous' timing, (in fact Blahous does not give exact figures) since the TRV shows a distinctive knee point.
- We use a different arc model and a different numerical technique.

So although it is possible to make the voltage injection circuit 'equivalent' to the direct circuit, this approach still leads to the least reliable results /45/ since the stochastic behaviour of circuit breakers /35,36/ has its influence on both the test breaker and the auxiliary breaker at the moment of interruption.

The voltage injection circuit will generally be more severe than the direct circuit, as was also concluded by Pflaum in 1965 /75/.

Case E. St-Jean et al.: Synthetic SLF test circuits

Another application of the Epa-method is the comparison of Short Line Fault (SLF) test circuits /46,47,48/.

Since especially the steep rise of the TRV during the first few microseconds in conjunction with the post arc current is critical in an SLF-test, the Epa-method is suitable for comparing the test circuits by means of arc circuit severity.

If we compare different Short Line Fault lumped element test circuits rated to ANSI >= 362kV (Z=360Ω, K=1.6) as defined by St-Jean et al. /49/ with a distributed parameter line, this results in:

Epa (Ws)	Line	RLC	nπ#3	nπ#4	KEMA 1.7
X-trans	**3.8130**	**3.8821**	**4.1420**	**3.8309**	**3.8114**
EMTP	**5.6781**	**5.6660**	**5.6784**	**5.6781**	**5.6790**

Table 2.7

The analyses were produced in a 362kV/60Hz direct test circuit with at the supply side a single frequency TRV shaping network and a simulation of a short line fault on an overhead line by 1) a Distributed line Z_ℓ=360Ω, 2)a RLC circuit, 3) a n.π#3(R=0.9Z) circuit, 4) a n.π4(R=Z) circuit and 5) the KEMA 1.7 circuit (circuits and parameters are given in Appendix I case E).

The Short Line Fault (SLF) had a Short Circuit Factor (SCF) of 91% (of 63kA) since this is within the critical range for SF6 circuit breakers.

In X-trans we applied an SF6 circuit breaker modeled with the KEMA model. The EPRI/EMTP v2.1 analysis was produced with an SF6 Urbanek circuit breaker model.

The relatively high Epa values indicate that a SLF thermally stresses the breakers to their limits, but the relative differences in Epa are small. All circuits produce equivalent thermal stresses in comparison with the distributed line model, except from the n.π#3 circuit, which might overstress the circuit breaker.

If we compare wave shapes, however, we see that the KEMA circuit and n.π4 produce the familiar saw-tooth wave shape, whereas the RLC circuit and n.π3 merely produce the first peak.

From this exercise it can be deduced that a good resemblance of wave shape (in the dielectric region mostly) is a preferable but not necessary prerequisite for a comparable thermal stress on SF6 breakers.

Even the very simple RLC circuit with only a few components produces an almost equal arc circuit severity and does not really overstress the circuit breaker, as published in /49/.

Case F. Urbanek: Severity ITRV and SLF

Another practical application is an Epa analysis of the Initial Transient Recovery Voltage phenomenon (ITRV) in the EPRI/EMTP v3.0.

The ITRV was added to the IEC-60056 requirements after it became obvious that in particular SF6 circuit breakers are sensitive to initial transient recovery voltages.
The ITRV has its roots in the investigations of Cigre WG 13.01 as published in Electra in 1976 /67/.
The IEC ITRV recommendations, as all IEC 60056 test recommendations, are based on the concept of an averaged inherent Network (Buswork) response, which does not include the circuit breaker influence.
As we know now, 'thermal severity' is related to both the network and the breaker and this is not in line with the IEC approach.

In combination with circuit breaker characteristics, this has been considered in /51,52/.

In the discussion of a paper by Dubanton /50/, Urbanek raises the question; "which is more severe: the ITRV or the SLF ?"

Therefore we will investigate:
1) whether IEC ITRV requirements are adequate and
2) whether the ITRV requirement is necessary when we test SLF separately.

In both cases the ITRV as well as the SLF the RRRV are directly related to the characteristic impedance of the circuit and the di/dt of the interrupted current.
The IEC network values, Z_{bus} = 260 Ω and 100% current, Z_{line} = 450 Ω and 90% current will be taken.

In order to give an answer to the question about the ITRV we will compare a direct test on a 245kV/40kA/60Hz circuit breaker as published in /37/ with the same circuit but modified for a correct IEC ITRV requirement.
The Epa values of the Urbanek SF6 Breaker model /42,43/ in the direct circuit and the direct circuit plus ITRV network will be compared with each other.

In order to give an answer to the second question the same breaker model is subjected to an SLF test (KEMA 1.7 circuit) in the direct test circuit.

The circuits are given in Appendix I Case F. Results of the Epa comparison are shown in table 2.8.

If we inspect the wave forms closely, the distortion discussed in /51,52/ shows up clearly.
Therefore care must be taken when the inherent response of a test circuit must meet the IEC requirements. This is difficult since each breaker modifies the wave forms in a different way.

	Direct	Direct + ITRV	Direct + SLF
Epa (Ws)	**0.00924**	**0.07116**	Failure

Table 2.8

From this table it becomes clear that a test with ITRV is much more severe than a test circuit without these requirements.
Therefore the IEC requirements are adequate on that point as different test stations can be compared in this way.

As the modeled circuit breaker shows a failure when subjected to the SLF duty, we can draw the conclusion that the SLF duty is more severe than the ITRV duty and therefore the thermal failure mode is best tested by an SLF test. A similar conclusion is drawn in /52/.

It would be too premature to abolish the ITRV requirements altogether, even though they are redundant when we consider thermal failure mode testing.
The ITRV requirement is valuable because it makes IEC and ANSI Breaker Terminal Fault (BTF) tests in different testing stations on SF6 Breakers more comparable.

On another level, to make small scale laboratory tests between one setup and the next more comparable, it was Frind who suggested that: "Future experiments should therefore be made with the deformations of current and voltage quantitatively defined." /66/.

Epa might be the tool Frind was looking for.

If we repeat the analysis with a slightly modified breaker model and another ITRV circuit (ITRV') which produces a ramp response instead of the

'1-cos' response produced by the π-section (please refer to Appendix I for details), we find the following results:

DIRECT	DIRECT+ITRV'	DIRECT+SLF	DIRECT+ITRV'+SLF
Epa = **0.00139632** Ws	Epa = **0.02332689** Ws	Epa = **0.08893605** Ws	Failure

Table 2.9

We see that the SLF test is again more severe in this computation than the ITRV' duty. A combined test with ITRV' and SLF circuits, however, produces an even more severe duty for this breaker.

Since an ITRV phenomenon always occurs in practice, it would be feasible to combine the SLF test duty with the ITRV requirements, thereby assuring that the breaker is in fact tested with the maximum thermal severity.

Case G.Weil-Dobke: injection frequency and timing

As another example of the use of Epa we will compare the classic Weil-Dobke synthetic test circuit /53,54,55,65/ with a direct circuit equivalent and table the changes in arc circuit severity (Epa) when within reasonable limits in order not to disrupt overall waveform equivalence:

- The trigger moment and
- The injection frequency are varied.

Varying these parameters influences the circuit breaker interrupting probability to a great extent as is published in /56,57/.

Direct circuit	**Weil-Dobke:** F_{inj} = 308 Hz $\hat{I}_{inj}$ on top I_{AB}=0 *Epa* = **0.002399** Ws	**Weil-Dobke:** F_{inj} = 308 Hz $\hat{I}_{inj}$ << I_{AB}=0 *Epa* = **0.001978** Ws	**Weil-Dobke:** F_{inj} = 308 Hz $\hat{I}_{inj}$ >> I_{AB}=0 *Epa* = **0.002377** Ws
Epa = **0.002537** Ws	**Weil-Dobke:** F_{inj} = 308 Hz $\hat{I}_{inj}$ on top I_{AB}=0 *Epa* = **0.002399** Ws	**Weil-Dobke:** F_{inj} = 264 Hz $\hat{I}_{inj}$ on top I_{AB}=0 *Epa* = **2.396E-05** Ws	**Weil-Dobke:** F_{inj} = 345 Hz $\hat{I}_{inj}$ on top I_{AB}=0 *Epa* = **0.019492** Ws

Table 2.10

This table was made with EPRI/EMTP v2.1 for a 245kV/50kA/50Hz SF6 circuit breaker Urbanek model, tested according to IEC-60056.
The circuits were taken from /21/ and are depicted in Appendix I case G.

For the base synthetic case: F_{inj} = 308 Hz and $\hat{I}_{inj}$ on top I_{AB}=0, the arc current di/dt was made equivalent in the direct circuit and the synthetic test circuit, i.e. $di_d/dt|_{t=0} = \omega\hat{I} \approx di_s/dt|_{t=0} = \hat{U}_c/L_i$.

As can be seen from table 2.10, the best equivalence is found when we choose a trigger moment such that the injection current reaches its maximum at the moment the auxiliary breaker (AB) interrupts.
Early triggering eases the arc circuit severity a little, whereas late triggering does not influence arc circuit severity significantly.

Therefore if triggering is difficult in practice and the additional arc energy (=arcing time) is not very critical, setting the trigger moment a bit late is a good solution.

For the injection frequency L_i was varied and it is clear that an equivalent di/dt as in the direct circuit is a necessity, otherwise the breaker is noticeably under or overstressed.

When comparing both influences we see that the di/dt is most critical and therefore tuning the circuit to the correct TRV-peak (related to the capacitor charge voltage) and inductance L_i in the injection circuit must be done with care. Early triggering is less critical but can better be avoided.

If we perform a similar analysis changing the injection frequency by changing the injection capacitance and keeping di/dt = $\hat{U}_c/L_i$ constant, we find;

Direct circuit *Epa* = **0.0092402** Ws	**Weil-Dobke:** F_{inj} = 420 Hz $\hat{I}_{inj}$ on top I_{AB}=0 *Epa* = **0.0076038** Ws	**Weil-Dobke:** F_{inj} = 350 Hz $\hat{I}_{inj}$ on top I_{AB}=0 *Epa* = **0.0080915** Ws	**Weil-Dobke:** F_{inj} = 500 Hz $\hat{I}_{inj}$ on top I_{AB}=0 *Epa* = **0.0069896** Ws

Table 2.11

This time, however, the analysis is done with the the EPRI/EMTP v3.0 testing a 245kV/40kA/60Hz SF6 circuit breaker modelled with the Urbanek-model. The circuits have been taken from /37/ similar as in case C.

From table 2.11 it can be concluded that a lower injection frequency (larger capacitor banks and therefore more charge Q = C.$\hat{U}_c$) is preferable to smaller capacitor banks with consequently higher injection frequencies.

From the results in tables 2.10 and 2.11 we may conclude that correct triggering is more relevant than the choice of the injection frequency, but the most important is a correct di/dt.

This is more strict than the IEC ruling that the injection frequency is to be kept within the range of 250 – 1000 Hz, whereby the period of the injection current should be at least four times longer than the transition period where significant change in the arc voltage is observed. Although this 'requirement' is based on a very sound line of reasoning by Rieder and Kuhn in 1961 /jj/.

Case H.Current deformation in a Weil-Dobke test circuit

Next we will investigate the influence of current deformation by the arc voltage /21,58,83/ on the thermal interrupting capability of a circuit breaker in a synthetic test circuit.

By comparing Epa values of a breaker model in a Weil-Dobke circuit as given in /21/ (refer to the circuit of case G in Appendix I).

In this circuit the ratio of the generator peak voltage ($\hat{U}_g$) to the sum of the arc peak voltages ($\Sigma\hat{U}_a$), so: $\hat{U}_g/\Sigma\hat{U}_a$, is varied.
In practice this ratio should be at least four (4) as stated in /1/.

The results are given in table 2.12

$\hat{U}_g/\Sigma\hat{U}_a$	33.74	19.85	9.92	7.00	5.00	**4.00**	3.00	2.00
Epa(Ws)	**0.007171**	**0.007125**	**0.007167**	**0.007164**	**0.007124**	**0.007081**	**0.007003**	**0.006899**

Table 2.12

Table 2.12 was made after calculations with EPRI/EMTP v2.1 using a Kopplin model for the Test Breaker (TB) simulating a 245kV/63kA/50Hz breaker with a peak arc voltage of $\hat{U}_a \approx 1425$ V tested for IEC Test Duty 4 (the arc model parameters are $K_t = 5.5^E-6$, $K_p = 2.0^E+6$ and [$V_{con} = 775$ V]).
The Auxiliary Breaker (AB) was modeled as an ideal switch and causes no arc voltage and no arc-circuit or arc-arc interaction.

The table shows that a voltage ratio less than four eases the interrupting conditions somewhat.
It must be said, however, that the thermal interrupting performance is not influenced much: 2,5% if the ratio is 2 instead of 4.
Above a ratio of four (4) the influence is negligible.

Since the EMTP arc models are not effective during the whole interrupting period, but only during a small time-interval /20,43/ around current zero, the above simulation does not include a full loop of current-distortion but only in a small time-interval around the current zero. This implies that the influence of the high-current arc-voltage on the current loop distortion /21,58/ is not fully developed at the moment of current interruption.

In X-Trans, however, an arc model is active during the complete simulation time-interval and therefore the full interaction between the high current arc and the circuit is taken into account.

If again we repeat the simulation of the TD4 test of a 'SF6' 245kV/63kA/50Hz circuit breaker model in X-Trans with a Habedank(/Browne)-model /61,62/ (in fact a series Cassie-Mayr model) with a high current arc voltage $\hat{U}_a$= 1 kV inserted for the Test Breaker and all other Breakers modelled as ideal switches, we get the following table:

$\hat{U}_g/\Sigma\hat{U}_a$	70.71	30.00	10.00	7.00	5.00	**4.00**	3.00	2.00
Epa(Ws)	**0.002595**	**0.002268**	**0.002140**	**0.002140**	**0.002084**	**0.001943**	**0.001949**	**--**

Table 2.13

Since the current loop is shortened under the influence of the arc voltage, especially for smaller ratios $\hat{U}_g/\hat{U}_a$, each trigger moment has to be adjusted such that the peak of the injection current coincides with the interruption of the auxiliary breaker.

Again we notice that the current distortion does not significantly influence the thermal severity of the Weil-Dobke circuit as long as the high voltage injection circuit is triggered correctly.

As in table 2.12 the Epa series of table 2.13 is not entirely monotonous since the injection moment has to be readjusted for every computation and for this computational exercise the arc-interval varies considerably because of the current deformation. Small deviations from the optimum injection moment cause small fluctuations in Epa.
Furthermore, since X-trans does not use a fixed time step as the EMTP does, the number of data points over which each integration is done to find Epa varies slightly. This causes another variation in the results.

Case I. Percentage SLF severity for ABB and GCB

Another area that can be investigated is the region of greatest sensitivity for a Short Line Fault for both Air-Blast circuit breakers (ABBs) and SF6 Gas filled circuit breakers (GCBs).

This is accomplished by inserting a distributed line segment (Z = 450 Ω) of variable length in a 245kV/40kA/60Hz direct circuit /37/ (refer for details to the circuit of case C in Appendix I) and tabling the Epa values as a function of the SLF Factor being $L_s/(L_s+L_\ell)$.

The circuit and circuit breakers will be simulated in the EPRI/EMTPv3.0 by an Avdonin model with parameters as used by St-Jean /26/ for an ABB and a GCB. The ABB has parameters:

A = 6.0^{E}-6, B = 1.6^{E}+7, α = -0.2, β = -0.5, [Vcon = 4200 V] and the GCB has parameters:

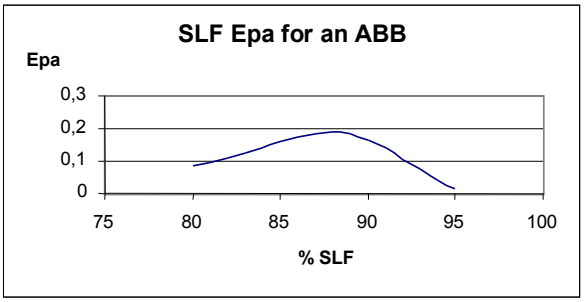
A = 1.3^{E}-6, B = 0.1^{E}+7, α = -0.15, β = -0.28, [Vcon = 500 V].

EPA (WS)	SLF=98%	SLF=95%	SLF=90%	SLF=80%	SLF=75%	SLF=60%
AVDONIN ABB	**4.309^{E}-05**	**0.0170465**	**0.1648142**	**0.0835060**	**0.0431646**	**0.0047103**
Avdonin GCB	**1.84^{E}-04**	**0.001109**	**0.000393**	**6.54^{E}-05**	**2.68^{E}-05**	**2.81E-07**

TABLE 2.14

HENCE WE SEE THAT THE CRITICAL LINELENGTH FOR A GAS CIRCUIT BREAKER IS INDEED CLOSE TO 95%, AND THE CRITICAL LINELENGTH FOR AN AIR BLAST BREAKER IS BETWEEN 75% AND 90% AS IS KNOWN FROM PRACTICE.

IF WE PUT THE EPA SERIES (WITH 1% RESOLUTION) FOR BOTH BREAKER TYPES IN A GRAPH WE GET:



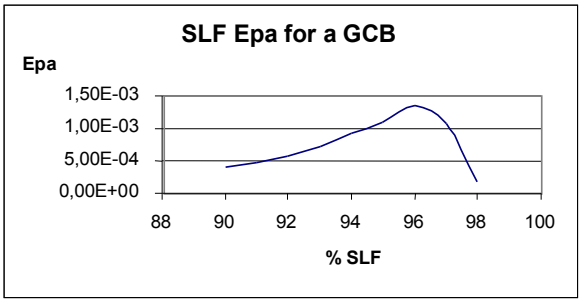


Fig. 2.6 SLF-Epa-series for an ABB and a GCB.

We see that the thermal sensitivity is related to the line length and has its maximum at a certain value for the line length. This effect is more pronounced for a Gas Circuit Breaker than for an Air Blast Breaker.

The point of maximum sensitivity is different for each specific extinguishing medium and type of circuit breaker.
So, testing a breaker according to IEC recommendations, like the 75% and 90% SLF tests alone could be insufficient.

It is understandable that IEC has chosen, as a compromise, only two fixed points on the line to test the ability of a circuit breaker of interrupting a Short Line Fault, but as can be clearly seen in figure 2.6 this approach is rather general.

A better approach would be to test a specific (type of) breaker for its most severe SLF-factor first, i.e. by means of digital testing, and then test the breaker (type) accordingly.

Or one might, as a compromise, test all SF6 breakers with a 95% SLF and all ABB breakers with a 85% SLF.

However, if we analyse a real SF6 Circuit Breaker like for instance pole B of the 145kV/31,5kA/60Hz Circuit Breaker tested by KEMA (see above), we find that the stochastic behaviour of the breaker could cause a single SLF-test to be too light in terms of thermal stress.

To prove this we will analyse the 145kV breaker to its rated values by means of a direct SLF-test. For each CB-model found for pole B, i.e. test #116 up to and including test #127 (see Appendix I table 3), we stress, by means of digital testing /76,81/ in the X-trans program, the new-KEMA-breaker-model (Kertesz-model) in a direct SLF-circuit for a range of SLF-percentages.
Since we are of the opinion that only a relative comparison between the CB-models of each test is relevant, the source side TRV is a 2-parameter TRV, in stead of the required 4-parameter TRV, however, with the prescribed RRRV and peak voltage. The 'short line' is simulated by the KEMA 1.7 synthetic SLF-circuit /48/.

The resulting relative Epa-values are a ratio of the Epa value for that particular test to the Epa-maximum for that SLF-series (see also /79/), for the 145kV CB are shown below, with a 1% resolution, in figure 2.7:

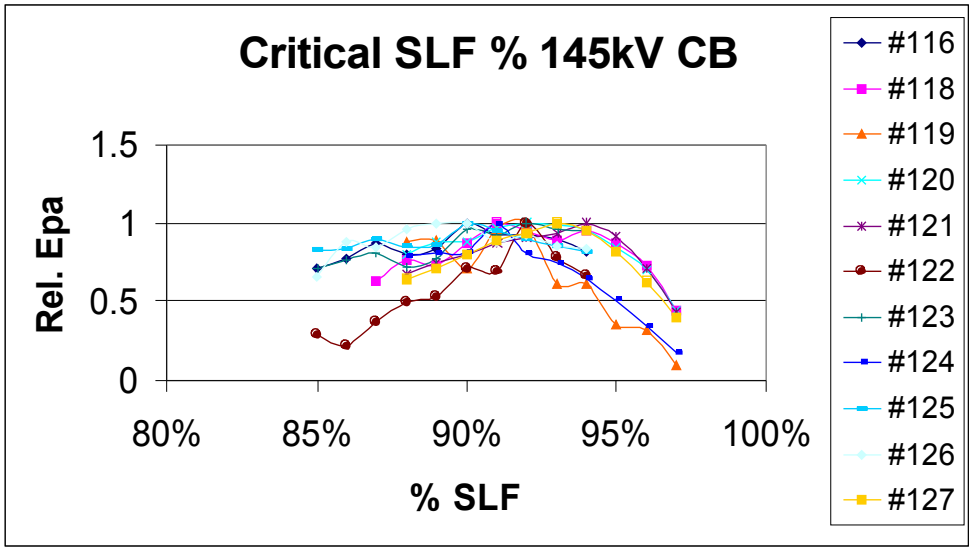


Fig. 2.7 relative SLF-Epa-series for the 145kV SF6 CB interruptions.

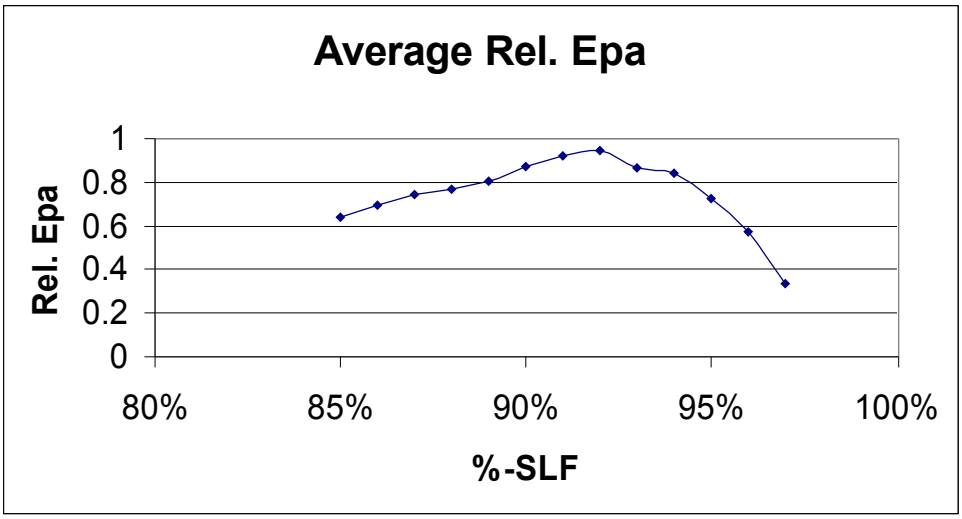


Fig. 2.8 Average relative SLF-Epa-serie for a 145kV SF6 CB.

From which we see that due to the stochastic behaviour the maximum stress percentage does vary from test to test, in this case between 89% and 94%. On average, however, 92% will be the most severe SLF test, as can be seen from figure 2.8.

Please note that the irregularities in the curves are caused by numerical approximations in both: the solution of the differential and algebraic equations (DAE's) and the use of the rectangular-rule for solving the Epa-integral, especially on sometimes only a few data-points.

Furthermore we see that, for this breaker, a standard 90% IEC test will not, on average, be far from the absolute maximum stress, since the curve is rather flat between 90% and 94%.

As to what is the best way of SLF-testing (most severe test), we come to the conclusion that one has to do more than one test for a SLF percentage which has been found, by means of digital testing /76,81/, to be the most severe for that (type of) breaker, e.g. 3 to 4 tests in a row. In this way the ageing process, which was found to be extremely influential, has also been accounted for next to the stochastic behaviour.

Case J. Schneider: passive parallel elements

As a last case we will investigate the best way how the interrupting cabability of an ABB and a GCB can be increased with the help of a parallel resistor and a parallel capacitor.

It is known from experience that the interrupting ability of ABBs is improved by a parallel resistor, but for GCBs a parallel capacitor is of more use /32,72,83/.

To show the influences we compare an ABB breaker model and a GCB breaker model, both simulated in X-trans by a pure Mayr-model.
For the gas breaker (GCB) we use τ = 0.5 μsec and P = 50 kW, for the air blast breaker (ABB) we use τ = 1.7 μsec and P = 250 kW as Mayr-model parameters.
The ABB model has been tuned to give some two amperes of post-arc current for about a twenty microseconds and the GCB has been tuned to give some 30 mA of post-arc current for about eight microseconds.

The test circuit is a conventional direct circuit with a voltage source of 100kV$_p$/50Hz, a current limiting reactor of 10 mH, and a TRV network with a 100 Ω resistor in series with a 10 nF capacitance.

Either a resistor of R = 500 Ω or a capacitance of C = 5 nF is put in parallel to the breaker.

The Epa results (units Ws) are tabled below:

GCB WITHOUT	GCB WITH R	GCB WITH C	ABB WITHOUT	ABB WITH R	ABB WITH C
0.000134595	**4.60990E-05**	**1.22977E-05**	**0.2971476**	**0.0637579**	**0.0866868**

TABLE 2.15

SO WE SEE THAT INDEED THE INTERRUPTING ABILITY OF A GCB IS BEST IMPROVED BY A CAPACITANCE AND THE INTERRUPTING ABILITY OF AN ABB IS BEST IMPROVED BY A RESISTANCE.
THE RESISTANCE IS HELPFUL AS IT REDUCES THE STEEPNESS OF THE TRV, THE CAPACITANCE IS HELPFUL AS IT ENABLES THE BREAKER TO DEFORM THE CURRENT

(REDUCING THE RATE OF FALL DI/DT) BEFORE ZERO AND IT DELAYS THE TRV BUILD-UP AFTER ZERO.

TO SHOW THAT IT IS A MONOTONOUS ARRAY IF EVER-GREATER CAPACITANCES ARE USED WITH A GCB AND A MONOTONOUS ARRAY IF EVER-SMALLER RESISTANCES ARE USED WITH AN ABB, WE HAVE VARIED THE CAPACITANCE AND RESISTANCE IN PARALLEL TO A GCB AND AN ABB RESPECTIVELY AND TABLED EPA RESULTS.

GCB	C= 0.1NF	C= 0.5NF	C= 1NF	C= 5NF	C= 10NF	C= 100NF	C= 1μF
Epa (Ws)	**0.0001271**	**8.819E-05**	**7.078E-05**	**1.688E-05**	**5.015E-06**	**-**	**-**
ABB	R= 10Ω	R= 100Ω	R= 300Ω	R= 500Ω	R= 1000Ω	R= 3kΩ	R= 10kΩ
Epa (Ws)	-	**0.0032310**	**0.0331525**	**0.0641551**	**0.1229533**	**0.2113963**	**0.2632291**

Table 2.16

Note 1: the dashes mean that the transient analyses tool (X-trans) could not solve the set of non-linear & linear differential and algebraic equations.

Note 2: the values for the data of the equivalent points in table 2.16 are slightly different as compared to table 2.15 because in table 2.16 a greater time step was allowed and therefore the solution is less accurate.

Please note that too small a capacitance or too great a resistor (compared to the amplitude and duration of the post-arc current) does not help the breaker significantly in the interruption proces.

2.7 Summary.

Circuit breaker test circuit severity and equivalence are difficult to define. A new parameter - dissipated post arc energy (Epa) - is introduced.

This parameter defines arc circuit interaction or thermal severity, for the whole interaction period, in a conclusive way.

It is possible to use Epa as a measure for circuit breaker ageing. This is shown in section 2.5.

In this section, using theoretical and practical / statistical means, it is shown that Epa is a good indicator for arc-circuit-interaction if we focus on arc models in network calculations.

Using Epa, it is possible to compare different circuits for the best ‘equal’ thermal severity or to find which circuit is the most severe for a specific (type of) circuit breaker. This is shown in section 2.6.

In this section, using many theoretical examples and based on experience published in literature, it is shown that Epa is a good indicator for arc-circuit-interaction if we focus on circuit topology.

With Epa we have a useful tool to quantify arc-circuit-interaction.

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3 CIRCUIT BREAKER ARC MODELS

3.1 Time-intervals in the interruption process of an electric arc.

When interrupting a fault current, a circuit breaker is generally stressed in four consecutive intervals /1,2,3,4,5/:
1. High current phase
2. Interaction interval
3. Dielectric recovery phase during TRV buildup
4. Dielectric withstand phase during TRV peak and RV.

These consecutive intervals are shown in Figure 3.1.

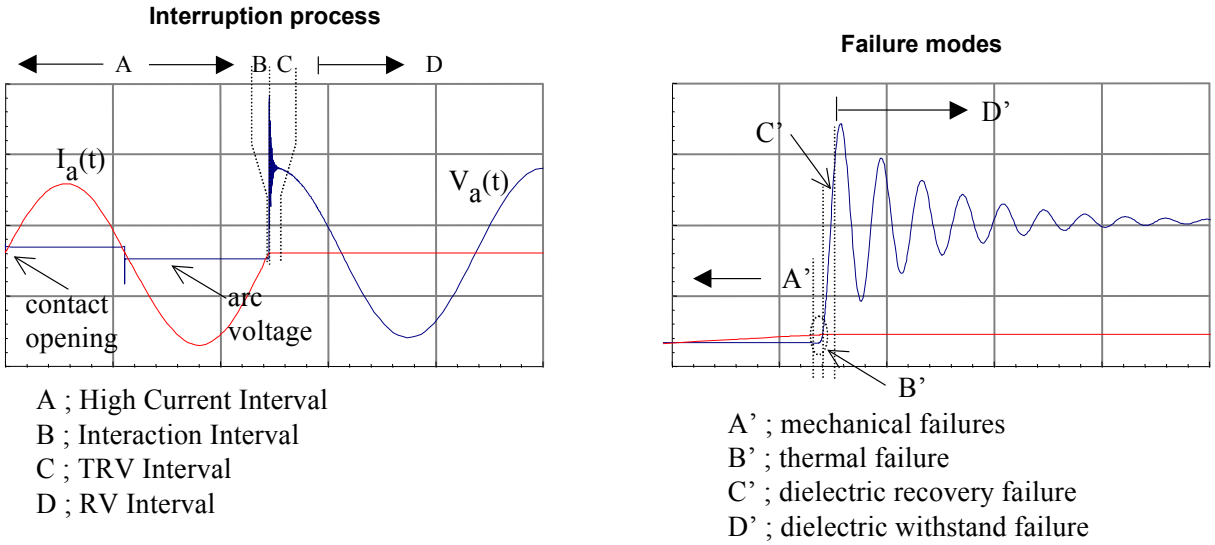

Fig. 3.1 Intervals and failure modes in the interruption process.

Each of these intervals has its own specific characteristics:
- high volume energy input into the arc which may cause the circuit breaker to overheat, explode or result in mechanical damage during the high current phase,
- arc circuit interaction with its related thermal stress and possible reignition in the interaction interval and
- dielectric stress which may cause a dielectric failure of the gap between the breaker contacts during the dielectric recovery and dielectric withstand period.

A three-phase-in-one-enclosure type circuit breaker (3PCB) experiences these same stress factors as an outdoor type (or life tank) circuit breaker but reacts in a different way because of the close proximity of neighbouring phases.

3.2 Arc models and their use.

In the previous chapter we discussed and used two-pole circuit breaker models as if it were an accepted way to do this.

Two-pole circuit breaker models have been in use for many decades. Their purpose is to model the electric Arc in a specific interval like the high current regime, the interaction interval or the dielectric recovery periods

in order to combine this model with network equations and to solve these simultaneously. This leads to conclusions as to whether the breaker is able to interrupt the current or to withstand the transient recovery voltage or not.

Over the years many models have been developed, each with their specific application.

For the moment we will focus on the so-called *black-box* or *phenomenological* models.

Because of their mathematical simplicity black-box models are commonly applied, since these models describe the high current phase and the interaction interval with a reasonable degree of accuracy and can therefore be used to analyze arc-circuit-interaction as supported by Cigre WG 13.01 in 1988 /6/ or to treat the problem of 'circuit severity' as already suggested by T.E. Browne, Jr in 1959 /36/.

All these models are an approximation of the conservation laws: balance in mass, momentum and energy.
And the most widely used 'Mayr'-type black-box models applied for arc-circuit-interaction analysis, are a sufficient approximation of the integral-boundary-layer analysis of the plasma arc /7/.

The derivation of the generalized arc equation is as follows;

The interruption process of high pressure (oil, air and SF6) arcs is predominately governed by plasma cooling. The cooling mechanisms are:

1. *Isentropic cooling*. Adiabatic expansion which occurs during the flow of plasma along the pressure gradient. It causes loss of internal energy and is represented by: $-\mathrm{div}(\rho u)$ (ρ = gas density, u = gas velocity).
1. *Cooling by thermal conduction*. This involves the transfer of heat due to a temperature gradient. It is represented by: $-\mathrm{div}[\kappa.\mathrm{grad}(T)]$ (κ = thermal conductivity, T = temperature).
2. *Cooling by mixing with background gas or convection loss*. This process is a result of the difference in temperature of the masses flowing in and out of the arc and is represented by: $+u.\mathrm{grad}(\rho h)$ (h = enthalpy).
3. *Cooling by radiation*. This cooling is the result of an energy flow in the form of radiation (light) which is radiated from the arc to its environment and this is mostly colder gas. It is represented by the function: $+R(T,\rho)$ (R is radiation in Watts).

Combined these cooling mechanisms form the energy conservation equation for a unit element of the arc at a certain moment in time t:

$$v_a(t)\,i_a(t) = \frac{dQ}{dt} - \mathrm{div}(\rho u) - \mathrm{div}[\kappa\ \mathrm{grad}(T)] + u\ \mathrm{grad}(\rho h) + R(T,\rho)$$

where $v_a(t)$ is the voltage over the unit's length, $i_a(t)$ is the current through the unit's area and $v_a(t)i_a(t)$ is the total power input into the unit's volume, dQ/dt is the change in the heat content Q of the unit element as time passes (for a certain temperature a unit element of plasma contains a certain amount of heat Q) and the other terms represent the different energy loss mechanisms from the unit arc element.

Under several assumptions the above energy equation can, for the *entire arc length* for a certain moment in time, be simplified to /37/:

$$P_i(t) = \frac{dQ}{dt} + P_o(t) \qquad \text{(Eq. 3.1)}$$

$P_i(t) = v_a(t) i_a(t)$ stands for the total power input into the arc and $P_o(t)$ stands for the total power output, i.e. all cooling mechanisms added, $v_a(t)$ now stands for the voltage over the entire arc, $i_a(t)$ now stands for the current through the entire arc and Q now stands for the total heat content of the entire arc. All at a certain moment in time t.

If we assume the arc conductance $G = i_a/v_a$ is a function of the heat Q stored in the arc at a certain time t then we can write for the arc conductance as a function of time:

$$G(t) = F[Q(t)] = \frac{i_a(t)}{v_a(t)} = \frac{1}{R(t)}$$

If we calculate the changes of the arc conductivity dG(t)/dt and substitute this in equation 3.1, this results in:

$$\frac{dG}{dt} = \frac{dF}{dQ} [P_i(t) - P_o(t)] \qquad \text{(Eq. 3.2)}$$

This is called the *generalized black box equation*.

The Mayr model /8/ can be derived from this generalized black box equation in the following way;

The conductance is taken as an approximation of Saha's expression /9/ for a gaseous equilibrium for a certain gas,

$$\text{Ln}\ \frac{x^2}{1-x^2}.Pr = -\ \frac{U}{aT} + b.\text{Ln}(T) - c$$

With; x: degree of ionisation of this gas
Pr: total pressure
U: heat of dissociation of this gas
T: absolute temperature in Kelvin
a,b,c: constants

It follows that,

$$\frac{x^2}{1-x^2}.Pr = \frac{e^{\frac{-U}{aT}} T^b}{c}$$

Under several assumptions this leads, for a mixture of ionized gasses, to:

$G = K.e^{[Q/Q_0]}$ with K and Q_0 being constants.

The power output P_o, assuming radial thermal conduction only, is assumed to be constant and the arc temperature varies linear with the arc channel radius.

The energy conservation equation can be written as:

$$v_a(t)\,i_a(t) = \frac{dQ}{dt} + P_o$$

and combined with equation 3.2 the change of the arc conductivity becomes:

$$\frac{dG}{dt} = \frac{G}{Q_0}\,[\,v_a i_a - P_o\,] \quad \text{and division by the conductance leads to:}$$

$$\left(\frac{1}{G}\right)\left(\frac{dG}{dt}\right) = \left(\frac{P_0}{Q_0}\right)\left[\frac{v_a i_a}{P_0} - 1\right]$$

$$= \frac{1}{\theta}\left[\frac{v_a i_a}{P_0} - 1\right]$$

This is the classical Mayr model where $\theta = Q_0/P_o$ is called the arc time constant being the time constant of arc cooling when the thermal input is zero.
The Mayr model is well suited for application around current zero /10/.

Arc models like the Mayr model, derived from the generalized black-box equation, are an accepted way to describe the energy balance in the interaction interval.

Browne and Frost made the following observation:
"Although physical analyses and careful measurements both indicate that their (Cassie and Mayr, AdL) *well-known parameters* E_0 (Cassie model, AdL) N_0 (P_0 in Mayr model, AdL) *and* θ *are never strictly constant, for an actual arc, these analyses and observations do indicate that during the brief critical time around current zero these parameters vary so much more slowly than the arc current or voltage that we are justified in assuming them to be momentarily constant."* /11/.

Many modern models are derivatives of the Mayr model, as can be read in /12/. The most used variation is that P_0 and θ are assumed to be a function of time, like the Schwarz-model /13/.

We will therefore use phenomenological arc models to analyze phenomena occurring in the arc-circuit interaction interval.

3.3 A historical Overview

The history of circuit breaker modelling goes back many years.

Already around 1900 static models were used that described the arc as a resistance which is an algebraic function of some parameters.

An example of this is the equation introduced by Mrs. Ayrton:

$$v_a = A + Bd + (C + Dd)/i_a$$

with v_a : arc voltage, i_a : arc current, d : arc length, and A, B, C and D constants. For copper contacts in air the constants are:

A = 19 [V]; B = 11,4 [V/m]; C = 21,4 [VA]; D = 3 [VA/m]

In 1905 the first dynamic arc model for a free burning arc in air was introduced by Hermann Th. Simon /a/.

Simon uses a model of the following form:

$$v(t)i(t) = (WTF)_t + L\left[\frac{d(TF)}{dt}\right]_t$$

with: TF being the product of the arc Temperature (T) and Area (F) of the cathode spot (to account for the momentary heat content of the Arc), W being the percentage of heatloss of the Arc at a heat content of TF and L being a constant dependent upon the contactmaterial, v and i are the arc voltage and arc current.

With this model Simon was able to get insight into phenomena observed for static and dynamic arcs, like reignition voltages, the time delay until reignition and the fact that open air AC-Arcs are more easily generated with contact material which has a low heat-conductivity constant (like Carbon).

But it was not until the late 1920s that serious work on arc models for circuit breakers was started by Cassie, Kopeliowitch, Mayr and Slepian /b/. This resulted amongst others in the classic papers by Cassie in 1939 /c/ and by Mayr in 1943 /d,e/.

Later more Mayr derivatives have been published and applied in practical cases.

A few of the most well-known are: the Browne model /f,j/ which is a combination of a Cassie and a Mayr model, the Hochrainer model /s/, a rather general equation or the Avdonin model /dd/ (θ and P_0 being power functions of arc conductance).

In the references of this chapter is a very extensive list /a – kkkk/, concerning circuit breaker modeling, given in chronological order.

The Mayr equation was also extended, as was done by Urbanek /w/ to take thermal non-equilibrium between electrons and ‘heavy’ ions into account /p/.

Others have taken a different route, like Rutgers /ooo/ who calculates the recombination of particles or Schoetzau /eeee/ and Verite /hhhh/.

Energy balance models are rather adequate to describe the high current and current zero regime, but for modelling the dielectric recovery and dielectric withstand period energy balance models are inadequate.

This is because the process of an arc column to its final cold, recombined state through temperature decay, chemical reactions and partial diffusion is characterized by processes for which local thermodynamic equilibrium (LTE) cannot be assumed /14/.

The deviations from LTE take the form of: non-equality of the electron distribution and heavy particle temperatures, non-maxwellian electron energy distribution, chemical non-equilibrium and demixing of various particle species /14/.

In order to describe this behaviour, one needs a rigorous solution of the conservation equations for mass, momentum and energy to get satisfying results when combining experiment and theory. An example of this approach is published in /xx/.

This is altogether rather complicated and requires, apart from fast computers, extensive experiments to give correct material parameters, boundary values and validation of the results.
These physical models always remain an approximation and can therefore never replace the experiment.

3.4 A model for three-phase arc circuit analysis

A 3PCB is subjected to similar stresses as a 1PCB, but the close proximity of the three phases in one enclosure makes those stresses more intense and stresses typical for a 3PCB have to be taken into account as well.

If we want to apply existing circuit breaker models, it has to be verified whether these two-pole simulations of the electric arc account for the extra three-phase effects or not.

In the *high current phase* the close proximity of the neighbouring phases cause the following extra interactions in a 3PCB which are not present in a 1PCB:

1. debris (hot and ionized SF6-gas) from a burning arc is exhausted between phases and the enclosure causing a significant reduction of the insulating properties in these areas.
2. gasdynamic cross influences of the neighbouring arcs results in forces from pressures on the arc itself.
3. magnetic cross influences make the arc move under the influence of the electro dynamical forces of the neighbouring currents.
4. three-phase gasdynamic effects exert a strong reverse mechanical force on the common parts of the three-phase operating mechanism.

One of the most important aspects of the high current phase is that it produces hot and ionized gasses which disturbs dielectric strength between phase conductors themselves and phase conductors and the enclosure /15,16,17/.

A 3PCB tested with a three-phase test method (3PTM) must sustain its rated short circuit current for the maximally possible arcing times because then it produces the maximum amount of debris. A 3PTM should give this high current stress and therefore the circuit breaker model must model the high current phase.

When the high current arc is examined more closely /18/, it turns out that it is a rather autonomous process. It is, for instance, difficult to interrupt the arc by a gasflow directed at the centre /19/ and for this reason it can be assumed that the influence of debris of neighbouring arcs on the *inner processes* of an unshielded high current arc is negligible.

A two-pole model can be applied to represent the arcing phases of a 3PCB in the high current interval.

Magnetic influences cannot be discarded because the magnetic fields are not ‘shielded’.

The influences of magnetic fields on arc behaviour are numerous and rather complex /20/. The Maecker effect that makes the arc unstable is one of them.

The influence of the magnetic fields on the interrupting ability, however, can be assumed to be of minor importance, as is reported in /15/.

Mechanical influences cause a large reverse force opposing the operating mechanism and thus cause a slower movement of the mechanisms during the opening operation.
The result is a reduced blow-out pressure for puffer-type circuit breakers, a longer arc time and a larger pole spread.
Therefore a 3PCB tested in a 3PTM must sustain its rated short circuit current for the maximum permissible arcing time to experience the maximum mechanical influences.

The conclusion is that a 3PCB-model simulating the interrupting performance as far as the high current phase is concerned, is not different from a model used in single phase simulations.

In the *interaction interval* everything is more complicated than in the high current interval.

First of all the arc model must be able to simulate a SF6 type circuit breaker with its specific characteristics, like a short arc-time-constant' and its often immeasurable small post arc current, since the majority of 3PCB's uses SF6 as an extinguishing medium.

Most phenomenological circuit breaker models are able to simulate the SF6 arc during the interaction interval to a certain degree of accuracy, as is discussed in section 3.2.

In the chapter on arc circuit interaction, it becomes clear that it is not realistic to disentangle the arc from the circuit and speak of typical arc or typical circuit contributions of the phenomena observed.

So choosing a different arc model or circuit breaker model gives a different result.

A way to deal with this problem is analyzing the thermal stress by quantifying Epa for different circuit breaker models in both the 3PTM and the 'real' network environment and compare the averaged results.

This is cumbersome because many different thermal stress evaluations have to be done with the circuit breaker models available in readily accessible form, this means already implemented in a Transient Analysis Tool.

Therefore, in order to simulate enough different arcs, an alternative is to vary model parameters over a defined range instead of making use of different models.

As a starting point we could use model parameters fitted onto real data of a successful interruption of a SF6 breaker (e.g. 245kV/50kA), preferably a 3PCB.
Next we can create a range of suitable circuit breaker models by changing the model parameters, thus covering a range of arc voltage extinguishing peaks and post-arc currents.

To account for specific three-phase effects in the interaction interval, we have to consider the electro-magnetic field interactions between phases with care.

Although Dubanton /22/ did not find cross phase influences for High Voltage 1PCBs to be of significance, in a three-phase GIS this can be quite different since Dubanton based himself on outdoor (life tank) type circuit breakers having a phase distance of at least one or two metres.

Other physical phenomena are considered to be too slow or their influence is too faint to be of influence in the interaction interval.

Electro-magnetic field interactions appear in capacitive coupling (the electric field component) and in mutual linkages (the magnetic field component).
Capacitive coupling and mutual linkages are directly related to physical dimensions.

Usually the dimensions of a 3PCB are too small and electro-magnetic coupling can be neglected.
But if we also include in our calculations the bus to which the 3PCB is directly connected, the physical dimensions necessary for electro-magnetic energy exchange between phases during the arc circuit interaction interval, are not negligible /21/. So in order to model the 3PCB during the interaction interval correctly we should add a realistic bus length.

The effect of the bus length is that by testing the 3PCB with all its normal components like current transformers and voltage transformers connected, ITRV phenomena are automatically included. This can be regarded as a real advantage since the ITRV regime can influence the interrupting capacity of a breaker to a great extent /22,23/.

However, as will be analyzed in chapter 4, the influence of the GIS bus length and the short lengths of connecting cables is that the thermal stresses caused by the steep initial transient recovery voltages are greatly reduced compared to a circuit breaker operating *without* a GIS-bus and *without* connecting cables.

And furthermore when testing for the thermal interrupting capability of a circuit breaker we will not need the extra bus length to be included in our model, or in practice during tests, because the extra capacitance is lowering the thermal severity (see chapter 2 example J or /35/ caused by the ITRV effects).

It is different for dielectric tests in the Laboratory, as it makes the tests more realistic adding this bus length from the viewpoint of insulation coordination because many three-phase bus systems have open connections to the circuit breaker compartments.

So a simple two-pole model inserted in one phase in a three-phase analysis does give, for the purpose of network comparison, a good simulation of the physical proces in the interaction interval.

The *dielectric recovery and withstand period* after current interruption is again a different matter.

When a circuit breaker pole has interrupted the fault current and survived the interaction interval, a race starts between dielectric strength of the gasious medium between the contacts and the rising Transient Recovery Voltage (TRV) /17,24/.

After this race the gap between the breaker contacts has to withstand the Recovery Voltage (RV) at power frequency /17/.

As discussed in section 3.3, dielectric recovery processes are rather complicated and require sophisticated physical models to simulate the phenomena.

This is not feasible for the research laid down in this thesis because we are not in a position to do extensive verification tests.

Therefore pure dielectric models will not be used but a few relatively simple black-box models include a kind of dielectric recovery failure mode: the Urbanek model /25/ and the KEMA model from Rutgers /26/.

The main difference between a 3PCB and its single phase equivalent lies in the fact that in the 3PCB hot and thin debris from still arcing neighbouring poles escaping from interrupting devices influences the dielectric strength of a pole which has already interrupted the fault current /15/.

This is especially dominant in the Recovery Voltage period when the poles of the interrupting device inside a 3PCB are uncovered.

For the Transient Recovery Voltage build-up phase it is of less consequence because 'hot' debris coming from neighbouring phases is cooled down much more than the gasses from inside the former gas column itself. This can be concluded from the experimental and theoretical investigations by Ragaller et al. /27/.

It is well possible that a TRV generated by one pole may cause a dielectric breakdown between poles or between a pole and the tank.

Furthermore, Recovery Voltages may cause a dielectric breakdown between poles or the tank (earth) because the influence of 'hot' and thin debris has a very 'long' time constant of about several **tens of milliseconds** /16,17/ and therefore it plays its tricks deep into the Recovery Voltage phase.

In order to simulate a dielectric withstand failure being a restrike during the TRV peak or RV regime, we would like to use a two-pole model which is capable of simulating both: a basic dielectric recovery failure and a dielectric withstand failure on a particular pole and, to account for three-phase effects, we would also like to have a tool for a dielectric withstand failure between phases and the tank.

This is possible with black-box models when we extend a two-pole model capable of causing a thermal failure and a dielectric recovery failure with a kind of flash gaps, over the pole itself and between poles and the tank, to be activated when a certain voltage level is exceeded at a certain moment in time.

However, this is rather complicated and gives us in fact only an indication that a set voltage level was exceeded.

In circuit breaker development this could be of use but in the development of a 3PTM a trigger event of this kind is of no practical value.

We will therefore use simple two-pole black-box models, capable of causing a (simplified) dielectric failure, to cover the dielectric phases.

3.5 Conclusion.

Summing up the requirements we could use either the Urbanek model /25,28/ or the KEMA model /26,29/, for the circuit breaker pole which is first to interrupt.

The Urbanek model is a standard circuit breaker model in the EPRI/EMTP versions since 1987 /30,31/[2] and the fact that it has been used in the past by other authors is a good reason to apply the model.

The Urbanek model is of the following form:

$$\frac{dg}{dt} = \frac{1}{\vartheta}\left[\left(\frac{\upsilon i}{e^2}\right) - g - \left(\frac{P_0}{e^2}\right)\left(1 - \left(\frac{\upsilon}{\upsilon_d}\right)^2 - 2\left(\frac{\vartheta}{\upsilon_d{}^2}\right)\upsilon\left(\frac{d\upsilon}{dt}\right)\right)\right] \qquad \text{(Eq. 3.3)}$$

with: υ = arc voltage in [V]
i = arc current in [A]
g = arc conductance (i/υ) in [S]

as its electrical variables

and: e = minimum arc voltage in high current phase in [V]
P_0 = minimum power input to maintain the arc in [W]
υ_d = dielectric breakdown voltage over cold arc gap in [V]
ϑ = arc time constant in [s]

as its model parameters.

Haupt /32/ concluded that Mayr derivatives of which the parameters (P, ϑ, etc) depend on electric variables (u, i and g) describe the SF6 arc with the best accuracy.

The Urbanek model fulfils this requirement but has, at first sight, fixed parameters only.
If we neglect the thermal unbalance term and rewrite Eq. 3.3 in the familiar Mayr form, we will find that both P and ϑ depend on g /25/.

The KEMA arc model is a standard option in another transients analysis tool: X-Trans /33/ and was also used in other studies.

This model is rather complicated compared to the Urbanek model since it has 5 parameters for the time up to current interruption and 11 parameters for the post-arc and dielectric phase.

The KEMA model passes the 'Haupt-test' too, because it has a cooling power which is dependent on arc current for the time up to current interruption.

A criticism, though, is that it is so 'filled with parameters' that it can be fitted with every conceivable (post-arc) voltage and current wave form /34/.

Another criticism could be that it has more than one differential equation which describes the complete interaction interval.

[2] According to Mahseredjian it only worked after he changed some of the original coding.

In the middle of this important interval the model switches from a modified-Mayr to a decay and recombination of particle concentrations. In order to make this work, an estimation must be made of the initial values of the concentrations of particles to be used, based on the value of the conductance in the modified-Mayr part of the model. This estimation is never as exact as a continuity analysis described by a single model.

Both models do include a kind of dielectric recovery failure mode but:
The Urbanek model is based upon a multitemperature Saha equation /9/, which is prone to give erroneous results /14/ and should therefore be interpreted with care.
The KEMA model has a rather simple dielectric failure mechanism, in that a certain critical field strength must not be exceeded (this restricts the calculation to a fixed arc length) and if it is exceeded the model simulates a dielectric failure, being a sudden breakdown of the arc resistance.

So, although dielectric failures are taken into account, the general use of this failure mode is not advised, but since both models fulfil our requirements for arc-circuit-interaction analysis, we will use either model, i.e. KEMA or Urbanek, depending on whichever transients program (X-Trans or EMTP) is the most appropriate for a specific circuit analysis.

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4 THE NETWORK, STRESSES ON 3PCBS AND THE STANDARDS.

4.1 Introduction

A circuit breaker operating in a power system has to cope with all kinds of stresses, especially when it has to interrupt a current, like short circuit currents, capacitive load currents and reactive load currents.

Short circuit currents usually create the most severe circumstances and therefore the name plate of a circuit breaker shows not only its voltage level but also the the maximum short circuit current that can be interrupted.

Short circuit currents can be divided into different categories, such as the Breaker Terminal Fault (BTF) and the Short Line Fault (SLF).

For the BTF and the SLF, IEC has defined special Test Duties (TDs) in order to be able to verify whether the breaker under test can interrupt these currents.

Current stresses are related to voltage stresses, being the different Transient Recovery and Recovery Voltages (TRVs and RVs).

Since different network topologies cause different TRVs, a generalized form for networks has been chosen /1,2,3/.

As we know now from the arc-circuit interaction discussion in chapter 2 and chapter 3, network topology and the arc itself do influence both di/dt and the rate of rise of voltage (dv/dt) around current zero and thus influence the interrupting capability.
Therefore inherent circuit stresses (created by an ideal circuit breaker without arc voltage or residual conductivity) are not realistic.

From the circuit breaker model discussion in chapter 3 we learned that three-phases-in-one-tank-type circuit breakers (3PCBs) have a more intense interaction with the network during the interaction interval and the dielectric phases, because of the proximity of the phases, than their single-phase counterparts.

The more or less generalized stresses formulated in IEC-60056, are not sufficient to adequately test 3PCBs.

To tackle this problem Cigre Working Group 13.04 has formulated five (5) additional requirements for synthetic tests /4/ and the IEC has issued a type 2 (open for criticism) standard /5/.
As far as we see it now these requirements result in a relaxation of the TRV and RV stresses 3PCBs are subjected to compared to real three-phase network stresses.

Although (single-phase) synthetic testing should be equivalent to direct testing and not to real network stresses as stated by Hochrainer in /6/, we feel that for three-phase synthetic testing, real network stresses must be analysed and taken into account.

This conclusion can be drawn since three-phase interaction is different from the transient recordings of switching conditions in networks of the past and different from the many Transient Network Analyzer studies which were the bases for the generalized TRV requirements for direct and

synthetic testing procedures as discussed in, for instance, /3,7,8,9,10,11,12/.

In those studies it was mainly dielectric stress that was looked at. Thermal stress, as we analysed in Chapter 2 and 3, came into the picture afterwards when a delay time /3/ and later an Initial Transient Recovery Voltage (ITRV) requirement /13/ was defined.

Furthermore, mostly first pole to clear TRVs were studied. Yet, in the chapter on circuit breaker models we noted that especially dielectric stresses between phases and phases to ground, i.e. second and third pole TRVs and RVs inclusive, play a key role for a 3PCB.

In order to find TRV stresses which can be coupled to certain network characteristics, we will first study different network topologies and their behaviour under ideal switching conditions with the use of ideal switching elements.

To describe network characteristics without including any of the effects of the circuit breaker itself, inherent network characteristics were chosen to be the basis for test standards during the 1930s /z/.
This was done on the grounds that:
"……if any breaker has the property through high electrostatic capacitance, arc drop, conducting properties after interruption, or any other incorporated scheme to reduce materially the severity of any test below the severity of the test circuit alone and in this way help to accomplish interruption, such a reduction will be credited to the breaker and the test record will state that the breaker has withstood the severity of the external test circuit."

This axioma was based on the theories of that time, such as the race theory (Slepian) or the wedge theory (Prince&Skeats, Kesselring), all of which dealt with the dielectric failure mode only.
The thermal failure mode, however, which – as we have seen in chapter 2 - has to take the physical behaviour of the circuit breaker into account as well, was not known at that time.

Therefore we will include the physical behaviour of the circuit breaker into the analyses by means of a circuit breaker model where applicable.

After we have established the network characteristics, as a second step, these networks are to be simulated by a lumped element 3PTM.

4.2 History of Transient Recovery Voltage (TRV) Investigations

In the 1920s it became clear that during interruption a circuit breaker was subjected to more than just power frequency voltages. One of the first extensive and clearly formulated papers on TRVs in power systems was authored by Park & Skeats /a/.

One of the things that played an important role in the discovery and analysis of the TRV was the introduction of the Cathode Ray Oscillograph (CRO) /y/.

Then the Transient Recovery Voltage (TRV), or Transient Restriking Voltage as the British used to call it, made it to the forefront of circuit breaker research.

Two items were investigated:
1. The relation between network topology and the TRV /a,b,c/ and
2. The response of the circuit breaker to the TRV /d,e,f/.

But quite soon matters were divided into different areas of interest such as circuit breaker development, testing and network behaviour.

Since all areas of interest are related, TRVs were subsequently investigated in other areas than network behaviour, like testing /g/.

An outstanding work on analytical Transient Recovery Voltage analyses is the work by P. Hammarlund /c/ in 1946.
Apart from giving an excellent analysis on general TRV characteristics, on which methods can be used for investigation, this work also gives an analysis of the Swedish Networks on all voltage levels in particular.

Hammarlund also discusses methods of defining the Rate of Rise of (Transient) Recovery Voltage (RRRV) and the conclusion can be drawn that this analysis must have led Hochrainer /h/ to his formulation of the four (4) parameter method to define TRVs.

Also a detailed outline of the history of TRV analyses is given, reviewing all publications dating back to 1919.
For those days this work is almost complete (it only fails to mention the Bergeron method /i/ which was published first in 1950 but already applied in 1931) and shows in great detail the progress in 'know-how' of Transient Recovery Voltage and its effect on circuit breakers.

By the end of the 1930s other equipment for the investigation of TRV proporties became available, namely the use of the calculating board or Transient Network Analyzer (TNA for short).

The TNA made it possible to study TRV responses of larger networks because of its method of simulating a network by means of lumped inductances, capacitances and resistances and small scale models of generators and transformers. Even multiphase systems with mutually coupled phases could be represented.

A well-known name connected to the early use of TNAs is: H.A. Peterson /j,k,l/.
The TNA has been used since by public utilities, industry and universities, but was made redundant by the digital computer /m/.

In the 1940s extensive studies – on the basis of calculations - into the general characteristics were carried out by the Association of Edison Illuminating Companies (USA), as is reported in /u/.

In the 1950s the Short Line Fault (SLF) came into the picture and for the sake of standardization an extensive World Wide Investigation into TRVs was undertaken during the 1960s /n/.

The fact that the SLF was unknown before the 1950s is described by Hammarlund in /c/ as he, for the definition on RRRVs, states that:
"Finally, if the first loop is abnormally low, it should be neglected, (fig 138 e). In fact, it has been decided to neglect the influence of loops with crest values lower than about forty per cent of the power-frequency instantaneous voltage. This approximation is quite arbitrary, although it has been shown by tests that there is some justification for it."

It was Hochrainer who classified TRVs by means of the so-called 4-parameter method /h/ and in 1971 the 'most severe' cases, coupled to the well-known

testing practices of 10%, 30%, 60% and 100% current rating, were defined as testing stresses in IEC-60056.

Together with the World Wide Investigation into TRVs during the greater part of the 1960s and started by Cigre, which was published in report 13-10 on the 1968 Cigre conference /n/, it was also analysed how to make 4-parameter TRVs in Testing Stations /o/.

This discipline has been more and more refined since then, e.g. /p,q,r,s,v,w/, resulting in the TRVs in use nowadays which follow the prescribed envelope with an extremely high degree of accuracy.

The logic behind this, though, is not quite clear since, as we will see in the Chapter on the 3PTM, current TRV 4-parameter wave-forms are not to the ultimate benefit of the dielectric testing value of such TRVs.

Another remark of caution on testing was made earlier by Urbanek /t/.
He stated that, since only about 1% of circuit breaker failures can be attributed to failing to interrupt at maximum capacity and for instance 84% is caused by mechanical failures, it will not improve the reliability of Circuit Breakers when tests to prove maximum breaking or making capacity are refined more and more.
This is confirmed in /x/ where an international study reports that of the small percentage of electrical failures, 90% is *expected* to switch off a current lower than 80% of rated short circuit current, but in fact the short circuit currents *in practice* are in most cases even lower than 20% of rated short circuit current.

In spite of the statements of Urbanek and others for 3PCBs it is a necessity to reexamine electrical test practices since 3PCB are a real departure from 1PCBs and so we have to find what constitutes three-phase worst-case TRVs for 3PCBs in particular.

Therefore we will now do an investigation into TRVs for the networks which exist today or are expected to evolve from present networks in the foreseeable future.

4.3 Common Network Topologies

3PCBs were developed to fulfil the power requirements set by modern urban societies such as in Tokyo, Japan.

In these cities, every square meter of surface area is used optimally and infrastuctural facilities are built underground /14/.

Especially the electric power consumption per square meter earth surface is rather high and requires therefore high voltage transportation levels.

The scarcity of land makes overhead lines and open air substations too costly, thus enforcing the use of Gas Insulated Substations (GIS) as nodes in a web of high voltage cables.

The scarcity of land in metropoles in combination with an increased power consumption pushed the immediate use of the premature new technology to build three phases in one tank type SF6 circuit breakers /14,15/.

It was then that engineers found that the application of three phases in one enclosure requires special attention /16/.

Considering this we realize that 3PCBs usually have to operate in a dense high power cable type network /17/.
They will be mounted in a GIS substation which has two or three feeders from an Extra High Voltage or Ultra High Voltage network and a few cables to other nodes.
The network topology will in general be radial /17,18/ as to reduce short circuit currents to acceptable levels and therefore meshed networks will be less common.
The average cable length is about 20 to 30 kilometers.

A voltage level 150kV is realistic /18,19/ and short circuit currents of 31,5kA cannot be far off practical values.
Power generation is in general not directly connected to such a GIS.

With 3PCBs being developed and their reliability proven in practice, they compete nowadays with their single-phase counterparts, not only in Cable Type Networks but also in more conventional networks and even more so in the near future.
That is in high voltage Overhead Line Type Networks connecting power plants and loads (cities etc.) all over the country.

When applied in such a network environment, we must consider that they are connected to the 'long' overhead lines by 'short' lengths of cable (up to some few hundred meters long).
Also a direct supply from a nearby power plant is likely to occur and current limiting reactors, common in the Cable Type Networks, will rarely be installed.

A voltage level of 300kV becomes normal and short circuit currents of up to 40kA should be quite common.

We will therefore analyse two types of network topologies:

- Overhead Line Type Networks (commonly having substations with direct supply from a power plant) and
- Cable Type Networks with substations mainly fed through two or more transformers.

4.4 Stresses in Overhead Line Type Networks

First we will investigate the conventional meshed, Overhead Line Type Networks.

Having done so we will investigate the more modern radial Overhead Line Type Network. This type of Network has evolved from the meshed type in urban areas such as Tokyo, Japan.

We will differentiate between thermal and dielectric stresses on the interrupting devices.

Because of their specific nature, Short Line Faults (SLFs) are discussed separately.

4.4.1Meshed Overhead Line Type Networks (MOLTN)

4.4.1.1.Dielectric stresses

When we compare the use of modern 3PCBs in the Meshed Overhead Line Type Networks of today with the types of networks investigated in the past /3,7,8,9,10,11/, we can conclude that there is not much difference between them, be it that three-phase GIS bus sections and short runs of cable were often not taken into account in previous TRV evaluations.

Although the difference in characteristic impedance between cables and overhead lines cause reflections which distort the form of the Initial TRV (ITRV), the overall shape (peak values and their phase relation), which is important for dielectric stress, will not be very much different from the shape of the TRV in a system without such short runs of cable.

The increased capacitance to earth, as compared to overhead line connections in an open air substation, predominantly causes an extra time delay for the TRV rise-time and this implicates that the thermal failure mode is affected mostly.

And, although increased capacitance causes an increase in the TRV amplitudes, this has a minor influence if we compare 3PCBs and their single-phase counterparts.

An increase in the dielectric inter-phase interaction through the coupling effect of these capacitances, in the usually effectively grounded (i.e. a ratio $X_0/X_1 < 3$) systems, is possible as well but has no great consequence.

And last but not least, a few short lengths of cable were taken into account when collecting and assessing data to define the standard (first pole to clear) TRV ratings as laid down in IEC-60056.

Therefore short runs of cable can be neglected when looking for the worst-case generalized dielectric Meshed Overhead Line Type Network switching conditions.

So, the TRV studies of the past, which resulted in generalized 2 and 4-parameter TRVs (IEC) or Ex-Cos TRVs (ANSI), cover the dielectric stresses to which a 3PCB is subjected when operating in a conventional network with open air substations and overhead lines.

This implicates that 2 and 4 parameter TRVs must be generated in a 3 phase test circuit.

The TRV tables in IEC-60056 (1987) only apply to the first pole to clear TRVs (across CB terminals). This pole has a so-called First Pole to Clear Factor (FPCF) which is usually higher than the Second and third poles to Clear Factors /20/.

For a 3PCB, TRVs across second and third poles to clear and between phases are at least as important as the First Pole to Clear TRVs but their form is not specified in IEC-60056 /21/ or IEC-61633 /55/.

When the second and third poles to clear Recovery Voltage (RV) parameters are in correspondence with their Pole to Clear Factor (PCF) and phase angle as in a three-phase direct test circuit, with identical TRV-networks for

all three poles, we can assume that they will automatically generate correct TRVs with respect to their peak and time to peak /21/.

When a 3PTM circuit lay-out with separate networks per phase to create the TRVs and RVs is used, we must make certain that the correct PCFs and phase relations between the first pole and the second and third poles to clear are met, since they are different for Non-effectively Grounded Systems or Effectively Grounded Systems /19/.

Another important aspect of a 3PTM is that correct (in amplitude and phase) Recovery Voltages (RVs) are applied to the 3PCB terminals for at least several *tens of milliseconds*, being several cycles at power frequency.

This is especially important since hot exhaust gasses (SF6) can diminish the dielectric strength between phases and to ground till 10% of its original dielectric withstand capability for several cycles of the power frequency, as measured and calculated in /16,21/.

Since a DC voltage might overstress the phase-to-phase and phase-to-ground (SF6) insulation /21,22/, an AC recovery voltage would of course be a natural choice for a 3PTM.

Another important aspect of a 3PCB is that in particular the transient voltages to the grounded tank are correct.
As was shown in /23/, the voltage gradient over the contact gap depends on several factors including the voltage to ground.
Therefore different dielectric behaviour regarding the withstand capability can be expected when the tank voltage is not fixed at ground potential.

In practice the tank of a 3PCB will be solidly grounded with many ‘short’ earth connections, with the result that, even during transients, the tank voltage rise will be low.

In a test station, however, it is practice to connect the objects between one another and ground through one well-defined connection. This is done in order to be able to measure the current to the station’s grounding system.

In fact hereby the tested object is connected to ground (for very fast oscillations) through a short transmission ‘line’ with a characteristic impedance and as a consequence the tank is lifted to a certain voltage level above ground during the transient period.

According to this reasoning it becomes clear that in a 3PTM in which the full voltages are applied to the poles, the tank of the 3PCB must be grounded solidly at the first place. Current measurements come second.

If, in a 3PTM, the voltages are applied partly to the poles and partly to the tank, by means of some kind of scheme to give the right voltages through proper voltage grading between poles and tank, care must be taken that all parts of the breaker have proper voltage stress as occurs in practice.

Because this latter boundary condition is rather difficult to fulfil, it is generally preferred to use a 3PTM in which the full voltages are applied to the poles directly.

4.4.1.2.Thermal Stresses

For thermal stresses the short runs of cable or the GIS bus-section to which a 3PCB is connected must be considered.

This, because they generate ITRV oscillations with a considerable thermal severity and must therefore be taken into account.

We will do this by analysing the influence on the thermal severity of the TRV wave-forms for every standardized situation, this means for every IEC Test Duty.

For the Test Duties: TD1 ~ 10% and TD2 ~ 30% of the maximum short circuit current rating, we must realize that these duties are mainly based on Transformer TRVs /3/.

These test duties have the highest Rated Rise Recovery Voltage (RRRV).

This is because it was found that the highest RRRVs are generated when a substation is fed by just one transformer or two transformers in parallel and no lines or cables are connected to the supply side of the breaker /3,7,8,9,10/.

This can be explained by the fact that parallel lines, which in a meshed type network account for a large part of the total short circuit current, cause a less steep TRV /3,7,9,24/ with their total characteristic impedance $Z_{tot} = Z_{line}/n$ with n the number of parallel lines, i.e.:

$$\frac{d\mathrm{TRV}}{d\mathrm{t}} = Z_{tot} \cdot \frac{di}{dt}$$

The short circuit currents are moderate for TD1 and TD2, because they are supplied by the transformers only and the short runs of cable generally do not influence the TRV since transformers are usually connected through a GIS bus extension and so no short cables are connected to the GIS substation; therefore TD1 and TD2 can be regarded as testing mainly the dielectric failure modes of a circuit breaker and not the thermal failure mode.

Therefore, there are no special requirements for the 3PTM for thermal stresses for TD1 and TD2 when Overhead Line Type Networks are considered.

For Test Duty 3 (TD3 = 60% short circuit current rating) and TD4/5 (= 100% short circuit current rating), the short cables could be of importance since most outgoing lines are connected to the substation supplying, in case of a fault, the higher short circuit currents.

Although they behave the same as lumped capacitance with its delay time, reflections (in the case that $Z_{line} > Z_{bus} \geq Z_{cable}$, which is usually true) can cause a noticeable ITRV /13/.

To account for this influence in a 3PTM for testing 3PCBs operating in a Meshed Overhead Line Type Network, one could choose out of the following possibilities:
1. Use a separate ITRV network for the higher Test Duties or
2. Rely on the SLF tests since they give the same thermal stress.

An SLF test (at 90% of maximum short circuit current for SF6 Breakers) produces fewer hot ionized gasses than a full TD4 test. But this difference is not of major importance for the thermal behaviour of the 3PCB as we will see in Chapter 5.

Keeping in mind the outcome of our analysis into the severity of the ITRV phenomena and the SLF phenomena in the discussion on Epa (section 2.3), the second option, counting on the SLF tests, would be a practical method and is therefore preferred.

Another important influence on the interruption process from short runs of cables, is that they let the arc distort the di/dt just before current zero due to the influence of the extra capacitance, subsequently lowering the Rate of Rise of Recovery Voltage dv/dt after current zero.

As we will now show, this eases the thermal stress exerted on the arc to such an extent that it more than nullifies the extra thermal stress caused by reflections.

To prove this fact we will now investigate a fairly simple single-phase example network as shown in figure 4.1a.

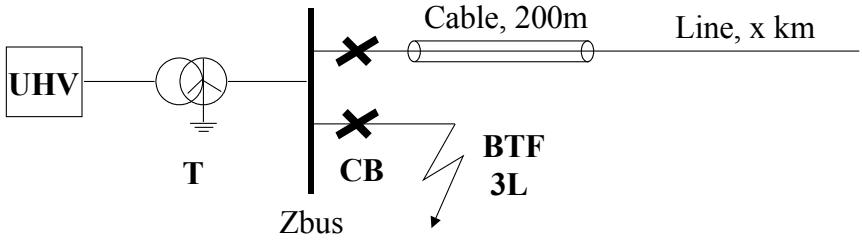

Fig. 4.1a Influence of short cable on thermal severity.

When we compare the thermal severity by means of Epa for a 1PCB operating in an open air substation (**without** the short (200m) cable and **without** Z_{bus}) with a 3PCB operating in a three-phase GIS substation (**with** the short cable and **with** Z_{bus}), we get the following result:

	1PCB; NO Z_{cable}, Z_{bus}	3PCB; Z_{cable}, Z_{bus}
Epa EMTP	0.00234 Ws	0.00000 Ws

TABLE 4.1 SINGLE AND THREE-PHASE SLF EPA COMPARISON

THE CB, SIMULATED BY AN URBANEK MODEL, WAS SET TO MODEL A SF6 BREAKER.

THE BUS WAS MODELED BY A 20M DISTRIBUTED 'LINE' MODEL WITH Z = 200 Ω. The cable was modeled by a 200m frequency-dependent L. Marti single phase cable model of a 150kV single core cable with Z = 80 Ω. The line was modeled by a 250km distributed line model with Z = 450 Ω.

From the table we see that the increase in thermal stress caused by the short cable (reflections) is nullified by the extra capacitance.

Even if we lower Z_{bus} to 80 Ω - this causes the first reflection to be positive - we find that the influence of the cable is such that the di/dt is reduced to very low values and the thermal stress is again Epa = 0 Ws.

So we can conclude that when testing a 3PCB according to IEC recommendations, thus like a 1PCB without bus and/or cables, conditions are

(much) worse than those a 3PCB will encounter when operating in a Meshed Overhead Line Type Network.

4.4.1.3.Short Line Faults

Under three-phase SLF conditions, a three-phase network alters the response as compared to a single-phase SLF situation to a great extent /25,26/.

The most noticeable difference is that, with every next pole to clear, the characteristic impedance Z_i of the short line length the circuit breaker pole 'sees', increases /28,29,30/.

The characteristic impedance (Z_3) encountered by the last pole to clear is composed of the characteristic impedance of the transmission line and the characteristic impedance of the ground loop: $Z_3 = \sqrt{L/C} + Z_e$ /28/.

If we simulate this situation in the EMTP with ideal Circuit Breakers for a three-phase 90% SLF (of 40kA_{rms}) for an untransposed length of a 230kV Overhead Line with a characteristic impedance Z ≈ 560 Ω in a grounded network and a earth resistance of R_f ≈ 1 Ω (see fig. 4.1b), it can be calculated that:

	FIRST POLE	SECOND POLE	THIRD POLE
DV/DT	8.4 KV/μs	7.2 kV/μs	8.3 kV/μs
di/dt	16.0 A/μs	12.8 A/μs	14.6 A/μs
Z_i	523 Ω	560 Ω	566 Ω

TABLE 4.2 THREE-PHASE SLF 'SEVERITY' PARAMETERS

THE CHARACTERISTIC IMPEDANCES ARE DETERMINED BY THE RELATION: $Z = \frac{dv/dt}{di/dt}$.

As we can see from Table 4.2, the first peak value cannot be calculated from the fixed characteristic impedance of the line (Z) only by the relation:

$v_p = Z_*(\omega\hat{I})*2\tau$ (τ the travel time between the CB and Fault),

because the di/dt differs per pole.

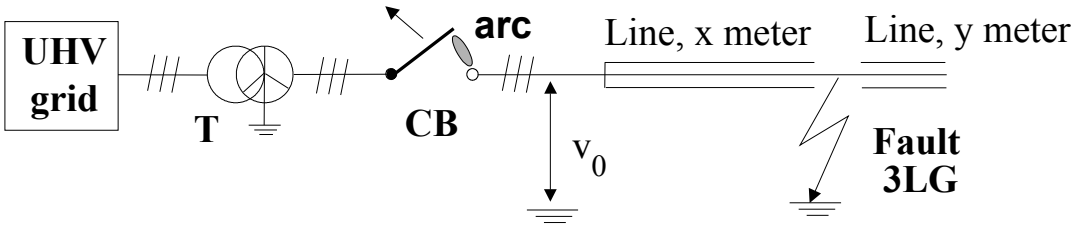

Fig. 4.1b Three-phase Short Line Fault.

For the first peak factor: $\sigma = v_p/v_0$, we derive from the numerical data:

	FIRST POLE	SECOND POLE	THIRD POLE
V_0	17334 V	48643 V	22459 V
v_p	40876 V	35121 V	40299 V
σ	2.358	0.722	1.794

Table 4.3 Three-phase SLF first peak factor

It becomes clear that a three-phase SLF is far more complicated compared with a single-phase SLF, for instance the peak factor of the 1st pole to clear is higher than 2 and may be as high as 2.7 /28,29/.

From Tables 4.2 and 4.3 we learn that the conventional parameters (dv/dt, di/dt, Z or V_p, σ) do not indicate clearly which pole suffers the most severe stress.
The first pole is severely stressed but also the third pole encounters an almost equally severe stress.

To establish which pole actually encounters the most severe stress, we will perform an Epa analysis by inserting an Urbanek circuit breaker model in the pole to be analysed and use ideal switches in the other two poles (table 4.4).

Epa 1st	Epa 2nd	Epa 3rd
0.0084833 Ws	0.0000000 Ws	0.0025363 Ws

TABLE 4.4 THREE-PHASE SLF EPA COMPARISON

THE REASON THAT WE FIND AN EPA = 0 WS FOR THE SECOND POLE TO CLEAR IS THAT THE INTER-PHASE CAPACITANCE REDUCES THE THERMAL STRESS BY ALLOWING THE ARC TO DEFORM THE CURRENT BEFORE CURRENT ZERO AND THE VOLTAGE AFTER CURRENT ZERO, AS CAN BE SEEN FROM THE FACT THAT DI/DT AND DV/DT ARE LOWER THAN IN BOTH OTHER PHASES.

THE FIRST POLE TO CLEAR IS THE POLE MOST SEVERELY STRESSED.

Although the above analysis holds good for a three-phase SLF, this situation does not occur very often in practical High Voltage Overhead Line Type Networks since the three-phase Fault is very rare indeed. The single-phase fault and therefore the single-phase SLF is much more likely to occur /24,31/.

In the case of a single phase short line fault in a three-phase system the two last clearing poles switch off unloaded or low loaded lines which is a mere dielectric stress, the circuit breaker is not significantly thermally stressed.

To find out if the first pole to clear in a single SLF is more or less severe than the first pole to clear of a three-phase SLF, we modify the circuit of fig. 4.1b such that the second and third poles switch off a capacitance equivalent to 200km Overhead Line. We find:

1ST 3ϕ SLF	1st 1ϕ SLF
0.0084833 Ws	0.0000000 Ws

TABLE 4.5 SLF FIRST PHASE AND SINGLE PHASE EPA COMPARISON

AGAIN, AS WITH TABLE 4.4 FOR THE LEAST STRESSED POLE, WE FIND A NEGLIGIBLE EPA BECAUSE THE URBANEK MODEL SHOWS A VERY 'STIFF' BEHAVIOUR, I.E. THE

RESULTING POST ARC CURRENT IS NEGLIGIBLE WHEN SEEN ON THE TIME SCALE (μsec) we are interested in.
'Stiff' should be seen as stiff for a beam, which is fastened at one end and bended by a force at the other but shows an almost negligible deflection because of its stiffness.

Table 4.5 shows that a full three-phase SLF is more severe and therefore this type of test must be the basis for SLF testing.

In practice the thermal severity of a Short Line Fault on a 3PCB operating in an Overhead Line Type Network will be reduced considerably by the influence of the short runs of cable because of the lower characteristic impedance and the capacitance of the cables.

Therefore a three-phase SLF test on a 3PCB not connected via the short runs of cable is a more severe operating condition and can be used to verify a 3PCB its ability to interrupt faults of this type.

The three-phase dielectric withstand capability of a 3PCB, can be tested best under BTF conditions /58/ such as TD4 and TD5, because the current is under SLF conditions lower.

Not only the current is reduced, but also the source side TRV peak voltage in the case of a Short Line Fault /32/, as can be calculated with the following (approximated) equation for the recovery voltage on the source side v_s:

$$V_s = \left(\frac{\sqrt{2}}{\sqrt{3}}\right) . V_n . \left[\cos(\omega .t) - \left(\frac{L_S}{L_1 + L_S}\right) . e^{(-t/\tau)} . \cos(\omega_1 . t)\right]$$

Hence we see that the peak voltage depends on the Short Line Factor:

$$SLF = L_S / (L_L + L_S) .$$

This leads to the conclusion that an SLF test is not suitable for testing the maximum dielectric withstand capability.

4.4.1.4.Covering for Meshed Overhead Line Type Networks in a 3PTM

If a 3PTM provides for correct TRV and RV stresses as defined by current IEC standards, with correct Pole to Clear Factors and phase relations for the second and third poles to clear, both thermal and dielectric stresses of Meshed Overhead Line Type Networks (MOLTN) can be considered to be covered as a result of the conclusions of section 4.4.1.1, 4.4.1.2 and 4.4.1.3.

Since most 3PCBs are not rotationally symmetric because distances between phases and to ground (tank) differ on a per-pole basis, it is important to use a test sequence such that every pole is successively the first, second and third poles to clear.

With such a procedure we make sure that every pole undergoes all possible TRV and RV stresses.

Other types of TRV stresses, such as the interruption of small inductive or capacitive currents, do not have to be analyzed and tested in a three-phase test circuit, although they can produce very high TRVs /33/.

This is because the arcing energy produced by these phenomena is much lower than in the case of a short circuit current interruption. So exhaust gasses are minimal in volume and do not affect interphase and phase to ground insulation strength in a 3PCB /21/.

Therefore the single-phase tests, as defined by current IEC standards, are sufficient for testing 3PCBs for those types of stresses.

4.4.2Radial Overhead Line Type Networks (ROLTN)

This type of network is not yet commonly used and therefore not widespread. As can be read in /17,18/ it has evolved from Meshed Overhead Line Type Networks in urban areas such as Tokyo, Japan.

Since it seems reasonable to expect that conditions leading to such type of networks, especially very high short circuit current levels, are not unique for Japan but prevail in many densely populated urban areas, we can expect to see the radial network structure evolve from the meshed network structure in the megapoles of the future. This means that networks are separated such that the radial structure remains, in order to reduce short circuit current levels.

The major difference between the meshed network and the radial network is, apart from their topological differences, that a substation in the radial network is mainly fed through a transformer bank of two or more very large transformers, instead of being supplied by the lines to which it is connected. This means that, in the case of a short circuit, the current is supplied by these transformers /17,18/.

The transformers, however, have high natural frequencies which are almost undampened /34,35,36,37,38/.

These natural frequencies cause a steep first excursion of the TRV, characterized in the standards by slope S_1, and a high peak value, characterized by peak factor γ /3/.

The higher the duty a 3PCB has to interrupt, the higher both values (S_1 and γ) may become, as was found in for instance /36/.
For CB standardization purposes this tendency was already foreseen as well as can be read in /3/.

The fact that these so-called transformer fed Transient Recovery Voltages (TRF TRVs) have high values of S_1 and γ is not restricted to any voltage level in particular but merely depends on the configuration of network elements, especially on the presence of TRFs in conjunction with lines and cables, since the phenomena were localized in Medium Voltage Networks as well /39/.

The reason for not taking this into account in IEC Test Duty 4/5 is that the more severe test duties in the past are related with network topologies in which the larger part of the short circuit current was supplied by Overhead Lines /3,7,8,9,10,11/ reducing the initial rate of rise and peak value of the TRV to a great extent because of the damping effect of the characteristic impedance (Z_{tot}) since:

$$S_1 = Z_{tot}.\frac{di}{dt} \qquad \text{and} \qquad TRV_p \approx \Delta V.\left[e^{-\left(Z_{tot}/L_{tot}\right).t} - \cos(\omega .t)\right]$$

With ΔV the driving voltage, i.e. the difference between the voltage that is the moment of interrupting the short circuit and the voltage that should have been without the short circuit.

In the IEC-60056 standard (1987) the influence of the transformer fed fault has been included in the higher values for S_1 and the peak factor γ for the smaller test duties, i.e. TD1, TD2 and TD3.
This is because in the Meshed Overhead line Type Networks a minor part of the total fault current in a substation is supplied by transformers.

In modern Radial Overhead Line Type Networks it is more the other way round.

In a ROLTN the higher short circuit currents (and therefore the higher test duties) could have higher values for S_1 and γ, whereas this compares to the smaller short circuit currents (and consequently the lower test duties) of the MOLTN, since the larger part of the total fault current in a ROLTN substation is supplied by large transformers.

4.4.2.1.RRRVs in Radial Overhead Line Type Networks

Although mainly the peak values of the TRV are of importance for 3PCBs and the Rate of Rise of Recovery Voltages (RRRV): S_1 and Initial peak: U_1 have no different significance as compared to 1PCBs, we will nevertheless investigate the RRRV for Radial Overhead Line Type Networks (ROLTN).

In literature /17,18,36,38/ reference values for the initial rise S_1 or Rated Rise of the Recovery Voltage (RRRV) are given.

When we compare averaged values of these references with the current IEC values for rated voltages of 300kV we get:

RRRV kV/μsec	~10% (TD1)	~30% (TD2)	~60% (TD3)	~100% (TD4)
Ref. /36/ 1970		5,4		
Ref. /17/ 1985	~5	~8	~3,5	~3
Ref. /38/ 1985		~8		
IEC 1987	7,7	5,0	3,0	2,0
Ref. /18/ 1993		~2	~4	~5

TABLE 4.6 RATE OF RISE OF RECOVERY VOLTAGES FOUND IN LITERATURE IN kV/μsec

From this we are able to conclude that, in order to cover for Radial Overhead Line Type Networks, the RRRV (S_1) for the 30%, 60% and 100% test duties should be increased.

Other parameters such as the first peak (U_1) must be changed accordingly, as will be shown further on in this chapter.

The 3PTM, therefore, must be able to produce the higher values for S_1 and U_1 for the test duties involved.

Based on the values of Table 4.6 we can deviate from current IEC values and propose:

- a RRRV = 7 kV/μsec for Test Duty 2 (30%),
- a RRRV = 3.5 kV/μsec for TD3 and
- a RRRV = 4 kV/μsec for TD4 and TD5.

However, in order to verify these values some cases of TRVs in a Radial Overhead Line Type Network in Section 4.6 will be investigated.

Based on literature and on results of numerical analyses, values that are able to cover the characteristics of Radial Overhead Line Type Networks are then proposed.

4.4.2.2.Peak of Transient Recovery Voltage in ROLTN

For the peak voltage (U_c) the analysis is not so simple, because the peak voltage depends on the amplitude factor γ as well as the First Pole to Clear Factor (FPCF),

$$TRV_p = FPCF.\gamma.\Delta V$$

With FPCF the First Pole to Clear Factor, γ the amplitude factor and ΔV the driving voltage, i.e. the voltage difference between the voltage at the moment the short circuit is interrupted and the voltage that should have occurred if no short circuit had occurred, i.e. steady state voltage.

When the amplitude factors from the references /34,36,37,38/ and IEC are compared for transformer fed faults for 300kV Transformers, we get:

REF.	/34/ 1968	/36/ 1970	/37/ 1972	/38/ 1985	IEC TD4 1987
γ p.u.	~1,8	~1,9	~1,8	~1,7	1,4

TABLE 4.7 AMPLITUDE FACTORS FOUND IN LITERATURE FOR TRANSFORMER FED FAULTS AT 300 KV TRANSFORMERS

From this it can be concluded that the amplitude factor for the higher fault current levels, i.e. higher test duties, should be increased. The values have to be corrected by a factor of 0.9.

For the smaller Test Duties TD1 and TD2 and the higher voltage levels IEC-60056 corrects this extra (amplitude) factor of 0,9 since during such faults in practice only 90% of the voltage drop is across the transformer and 10% is across the feeding network.

This mechanism is explained by Wagner in /40/ as a consequence of the fact that, for a fault fed by a transformer, the 'driving' voltage for the TRV is the voltage across the transformer (V_t), since the frequency $\omega = 1/\sqrt{LC}$ of the transient between the system inductance (L_s) and the system capacitance (C_s) is much lower than the natural frequency of the transformer ($C_s >> C_t$, although $L_s \approx 0.1 * L_t$).

For this reason the actual amplitude factor for those test duties, Transformer fed Faults, is corrected ($\gamma_{eff} = \gamma * 0.9$).

The First/Second/Third Pole to Clear Factors (F/S/TPCFs), however, depend on the construction of the transformers and the characteristics of the supplying Network as can be concluded from the following formulae for solidly grounded Networks /20/:

$$FPCF = \frac{3k}{1+2k} \quad ; \quad SPCF = \sqrt{3}.\frac{\sqrt{k^2+k+1}}{2+k} \quad ; \quad TPCF = 1$$

From these expressions we see that k = X_0/X_1, being the ratio of the zero sequence reactance and the positive sequence reactance, influences the Pole to Clear Factor significantly.

For Faults with earth return, like Single Line to Ground fault (1LG), X_0 (or more general $|Z_0|$) is considerably larger than X_1.

For this reason IEC introduced the value of 1.3 ($X_0 \approx 3.X_1$) for Networks of 245kV and higher because they are in most cases effectively earthed.

For Radial Overhead Line Type Networks the lines are relatively short, approximately 40 km, and then the influence of the generators and the transformers for which usually $X_0 < X_1$, starts to play a significant role. This is especially the case for large generators and transformers.

The situation can arise that the total X_0 is at least equal to - or can be even smaller than - the total X_1 /18/.

This results in a First Pole to Clear Factor ranging from 0,8 to 1,2 /18/.

The peak voltage for a 300kV system results in:
Peak voltage = 1,3*1,4 = 1,82 p.u. for the Meshed Networks (based on IEC values) and
Peak voltage = 1,0*1,8*0,9 = 1,62 p.u. for transformer fed faults in Radial Networks.

So the peak voltages in Radial Overhead Line Type Networks are in general equal to but can also be lower as defined in IEC.

Therefore, where the peak voltage in Radial Overhead Line Type Networks is concerned, we expect that a newly defined 3PTM does not have to do anything significantly different from what is currently defined in IEC standards.

For Not Effectively Grounded Systems (NEGS) that are grounded through a reactance or Networks with an Isolated Neutral, as is often the case for Overhead Line Type Networks of a rated voltage of 170kV and below, the standard IEC value FPCF = 1.5 should be applied.

4.4.2.3.Asymmetrical Short Circuit Currents in ROLTN

In Radial Overhead Line Type Networks the short circuit currents to be interrupted usually contain a DC-component, as is common for many parts of the power system.

The value of the DC-component depends on the phase angle of the supply voltage when the fault occurs.

The expression for the short circuit current can be written in the form:

$$i_k(t) = -\left[\frac{E_m}{\sqrt{R^2+\omega^2L^2}}\right].\sin\left(\phi - \tan^{-1}\left(\frac{\omega.L}{R}\right)\right).e^{(R/L).t} +$$

$$+\left[\frac{E_m}{\sqrt{R^2+\omega^2L^2}}\right].\sin\left((\omega.t)+\phi - \tan^{-1}\left(\frac{\omega.L}{R}\right)\right)$$

In this expression $v(t) = E_m * \sin(\omega t + \phi)$ is the driving voltage being equal to the sum of the electromotive forces of the synchronous generators, R the sum of the resistances in the circuit, including the fault, and L the total reactance of the circuit (synchronous reactances, leakage reactances of the transformers etc.).

For most circuits it can be assumed that $R << \omega L$ and $i_k(t)$ simplifies to:

$$i_k(t) = \frac{E_m}{\omega . L} . \cos(\phi) . e^{-\left(\frac{R}{L}\right).t} - \frac{E_m}{\omega . L} \cos(\omega t + \phi)$$

From this expression it can be easily seen that the ratio $\tau = L/R$ is the time-constant of the DC-component.
A fully asymmetrical current flows when $\phi = 0°$, or in other words when the voltage is zero at the moment the fault occurs.

With modern fast detection relays and installed fast 3PCBs the total time between fault initiation and the moment of contact opening is usually between 80 to 100 milliseconds.

In dense high power networks /17/, i.e. Radial Overhead Line Type Networks, the time constant of the Network is in the same order of magnitude /18/.

Although such systems are not widespread yet, they have been identified /41,60/.

In the power systems of the past, on which the IEC is based, the time constant is fixed at 45 msec and the time between fault initiation and first contact opening was assumed to be in the range of 100 to 150 msec.

After 100 mses the DC-component has then damped out:

DC-component = exp[-100/45] ≈ 0,108 p.u.

In dense high power networks, i.e. Radial Overhead Line Type Networks, as is the case in Tokyo, Japan /18,41/, detection relays and circuit breakers are fast, and the DC time constant τ has increased because:

1) cross sectional area of conductors has increased, so the line inductance has increased /18/ and consequently the time constant τ increases,
2) the percentage of the contribution to the short circuit currents of large transformers having a long time constant themselves has increased /18/ and therefore the overall time constant will rise and
3) generators feeding the fault will be relatively near, usually within 20 to 30 km. So generators, because of the specific generator characteristics like the symmetrical steady state short circuit current I_k being considerably smaller than the initial symmetrical short circuit current I_k" (or I_k') /42/, will play a more dominant role.

The time constant for Radial Overhead Line Type Networks can therefore exceed the value of 100 msec /18,41/.

For further analysis the time constant is taken to be τ = 100 msec.

For a CB that starts to open its contacts 60 msec after the initiation of the fault, the DC-component has the value:

DC-component = exp[-60/100] ≈ 0,549 p.u.

This is considerably more than official IEC recommendations for TD 1 to 4, requiring DC < 20% for circuit breakers that do not have to operate 'in the vicinity of centres of generation'.
The DC-component causes considerably more extra energy to be developed in the CB during the high current phase but also extends the arc-times. This causes more hot gas to be introduced into the free space between phases and tank. This reduces the dielectric withstand capability for a great deal and a 3PTM must therefore allow for these stresses.

Another aspect is that in effectively grounded systems the interruption of an asymmetrical current causes, between phases, a few percent higher TRV peak values as compared to the symmetrical case /43/.

Only creating an asymmetrical current in a direct test circuit with a high enough DC content is not sufficient since at current interruption the breaker experiences a much lower di/dt /44/ and that affects the thermal stress considerably.

In a synthetic test circuit with a parallel current injection Weil-Dobke the right current stress during the high current interval could be made by supplying a current from the current source with a sufficient DC content, see for instance /44,45/.

The correct thermal stress, in comparison with symmetrical short circuit currents, is subsequently supplied by injecting a current with a correct di/dt for that interaction interval.

4.4.2.4.How to cope with ROLTN in a 3PTM

Summing up the conclusions for Radial Overhead Line Type Networks it can be stated that a 3PTM should:

- allow for higher RRRVs especially for the test duties 4 and 5
- generate the same peak voltages as prescribed in IEC and
- allow for a high DC component in the current without reducing the thermal stresses in the interaction interval as a whole.

Therefore values for RRRVs and DC-content which deviate from current IEC values when rated voltages are 245kV or higher should be applied. Other parameters can then remain the same as they are in current IEC standards.

4.5 Stresses in Cable Type Networks (CTNs)

As analysed before, Cable Type Networks cause a different voltage stress on a circuit breaker as Overhead Line Type Networks do.

An important difference is that usually shunt reactors are installed to compensate capacitive load currents, thus balancing the voltage profile in the network.
Commonly the shunt reactors are installed at each end of a cable.

Shunt reactors cause extra problems in the case where load currents or unloaded cables are to be switched /46,47/. In cases where short circuit current are interrupted they hardly influence the TRV.

Another noticeable difference is that the Rated Rise of the Recovery Voltage (RRRV) is lower in cable networks than the RRRV in Overhead Line Type Networks.

The characteristic impedance of underground cables (Z_{cable}) is roughly 10% of the characteristic impedance of overhead lines (Z_{line}), so:

$$RRRV_{cable} = \frac{d\mathrm{TRV}}{dt} = Z_{cable}.\frac{di}{dt} = 0.1*Z_{line}*\frac{di}{dt} \approx 0{,}1*RRRV_{line}$$

A less noticeable difference between Cable Type Networks and Overhead Line Type Networks is that, although the RRRV is lower in Cable Type Networks, the peak value of the TRV can be higher /48,57/.

In order to quantify TRV stresses for 3PCBs in a Cable Type Network, a network is calculated with EMTP, and to be able to do so a representative basic substation layout is used and is varied in its topology:
with all cables connected, just one cable connected, etc.

This is an accepted method and was used before in studies, e.g. /9,10/.

Such an analysis cannot cover all possible topologies and cases of course, but is merely to indicate the differences between Overhead Line Type Networks and Cable Type Networks.

If a more complete analysis is required, an investigation should be carried out for Cable Type Networks, as was done in the 1960s for Overhead Line Type Networks /3/.

4.5.1Substation Layout

Literature studies /9,10,15,46/ show us that a typical substation layout consists of:

- Three ties (cables) to neighbouring substations, each between 20 to 30 kilometers long.
  In general the neighbouring substations are fed by our main substation and do not have/use their own supply from the grid;
  the Cable Type Network has a radial topology.
- Two or more supply transformers that (redundantly) feed the substation from, for instance, a 300kV Overhead Line Type transmission network.
- Two or more step-down transformers supplying distribution networks (for instance 50kV).
- At least one shunt reactor, to compensate the cable capacitances, that is connected through its own separate breaker.
- A double-bus system with one coupler in order to be able to connect or to separate both busbars of the substation.

A typical substation voltage level is 150kV and a nominal short circuit current level is 31,5kA.

The Cable Type Network will usually be a Not-Effectively Grounded System (NEGS). NEGS implies that the neutral is connected to earth through a high impedance or isolated.

Fig. 4.2 depicts the single line diagram of a typical High Voltage substation:

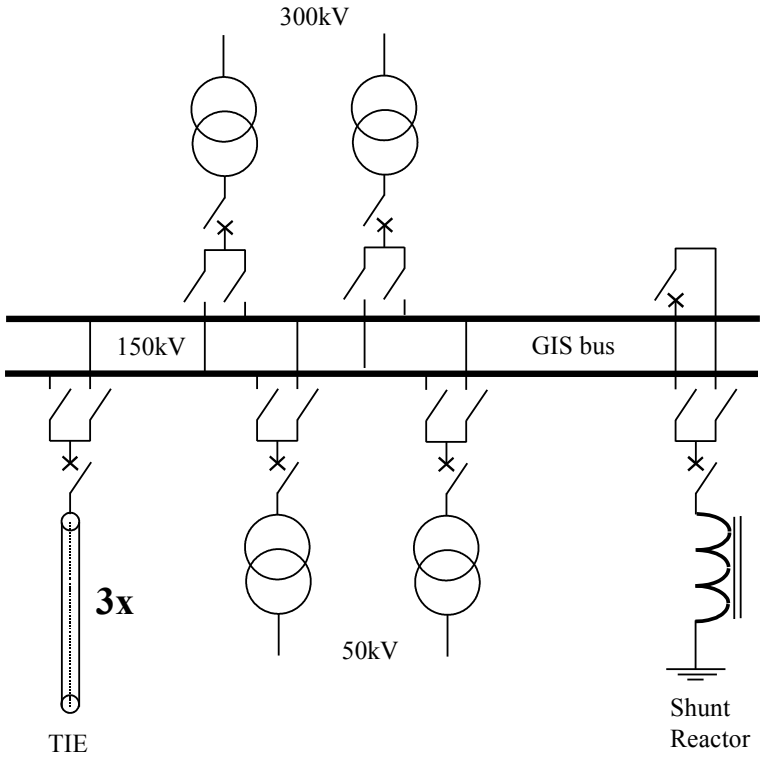

Fig. 4.2 Single line diagram of a 150kV High Voltage substation.

The following situations will be investigated for this substation:

a) Maximum short circuit power, with all supplying sources connected to the substation and a short circuit occurring directly behind a tie breaker. This complies with IEC-60056 Test Duty 4.
b) Again maximum short circuit power, however, only the 300/150kV supply transformers are connected to the bus and a short circuit occurrs directly behind the only remaining tie breaker. This should also be covered by Test Duty 4 of IEC-60056 and is therefore called the 'alternate' TD4.
c) Supply from one 300/150kV transformer with no cables or step-down transformers connected and a short circuit on the 150kV busbar. This complies with IEC Test Duty 3.
d) Supply from one tie and one step-down transformer (150/50kV) only connected. Short circuit on the 150kV busbar.
This complies with IEC TD 1/2.

In order to investigate the influence of the shunt reactor a few situations are analysed with the reactor connected and disconnected.

Although most of the short circuits will start as phase to ground fault, it can be readily assumed that, by the time that the fault is detected and successfully interrupted, the fault will have developed into a three-phase fault.

This is basically different from Overhead Line Type Networks where the three-phase fault is a highly unlikely event (according to Schramm in the discussion of paper /24/ and supported by Russian /31/ and German statistics /59/) but was taken as the most severe fault situation /59/.

Higher TRVs in case of two-phase ungrounded faults can exist, but are not likely to occur in practice /10,49/ and apart from that still result in a less severe stress between phases and between phases and earth in the case of a three-phase Breaker Terminal Fault (BTF) /19/. A quote from /50/: "The most severe recovery conditions for such 3-phase circuit breakers occurs under breaker-terminal fault interruption. Under such conditions the arc current, the arc-injected energy and the recovery voltage between phases are greater than for all other duties such as short-line fault and out-of-phase interruptions."

For the cases a), b), c) and d) the 4-parameter envelope will be determined and the 4-parameter TRV envelopes for the first pole to clear are compared with the envelopes as defined in IEC-60056 for the test duties that correspond with the examined cases.

4.5.2System representation and substation equipment modelling

A choice must be made as to how detailed the supplying high voltage network (in out example 300kV) and the connected distribution networks are modeled.

Diesendorf et al. /48/ gives practical guidelines on how detailed the models have to be.

How detailed lines, cables and discontinuities that are not directly connected to the main busbar must be represented, is governed by the fact that network studies have shown that in most cases the TRV reaches its peak within 2 milliseconds (msec) after current interruption /8,48/.

This implicates that the reflection of waves against discontinuities and transformer windings of which the travel time for a round trip exceeds 2 msec do not have to be represented in detail (1 millisecond equals approx. 300 km when travelling with the speed of light).

Also the amplitude of the cosine wave of the supply voltage towards which the TRV oscillates decreases /48/ and after 2 msec this amplitude is reduced by approximately 19% at 50Hz.

For Overhead Line Type Networks this fixes the boundary at approximately 300km and for Cable Type Networks discontinuities at 100km can influence the peak value of the TRV.

Note that for cables the wave velocity is roughly reduced to 1/3 of the wave velocity for lines, which is slightly below the speed of light in vacuum (~3.10^8 m/s).

But in the majority of cases the peak is already reached within one millisecond after current interruption. This brings the boundary for modelling at some 150km for Overhead Line Type Networks or 50km for Cable Type Networks.

Care must be taken that the fault currents supplied by local ('lumped') sources are represented correctly. These currents, even if they are relatively small, do influence the Initial TRV over the Rate of Fall of Current (di/dt) and subsequently the initial rate of rise of the TRV:

$$RRRV = \frac{d\mathrm{TRV}}{dt} = Z_{tot}.\frac{di}{dt} \approx Z_{tot}*\omega\hat{I} \qquad \text{for small values of t.}$$

The measure into what detail passive network components must be modeled is set by the voltage difference (ΔV) between the voltage at the moment of interruption and the steady state voltage that must result, within the boundaries set by the round trip reflection criterion.

This is because the TRV is directly dependent on this voltage difference. The voltage profile during a short circuit between the source(s) and the fault determines into what detail parts of the system should be represented.

Example:

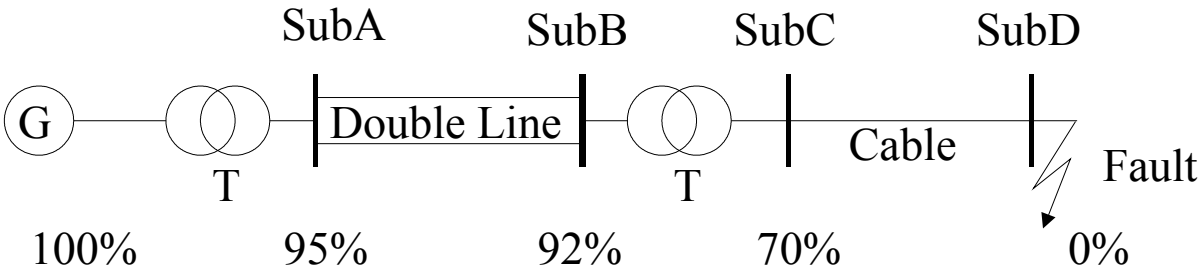

Fig. 4.3 Voltage profile along the fault path.

From the voltage profile along the supply path we can see that the voltage difference ΔV is the greatest in D, that is a 100%.

The TRV-peak is directly related to this voltage difference:

$$TRV_p = FPCF.\gamma.\Delta V$$

and it is clear that substation D, having the breaker that is to interrupt the fault, must be represented in detail.

Substation C, with a ΔV of 30%, can be represented with less accuracy and substations B and A will not noticeably influence the TRV at the breaker terminals, in D that is.

It is understandable that we must represent the substation itself as accurate as possible.
This means that all elements directly connected to the substation should be modeled to result in a realistic transient behaviour /13/. This will be discussed hereafter.

The supplying network, however, can be represented by a simple infinite bus feeding the network over an overhead line modeled by a distributed parameter model.

The outgoing 50kV cable distribution networks must be taken into account as a lumped capacitance, connected to the substation through a transformer /48/.

Also loads for the voltage levels to be investigated have a noticeably damping effect on the TRV /48/, therefore they must be included.

The substation itself, as described in the previous section, consists of equipment that must be represented with adequate precision in order to result in the correct transient response.

Initial TRV (ITRV) effects /13/, taken into account through the modelling of Current Transformers (CTs) and Voltage transformers (PTs) etc., can be omitted since the ITRV influences thermal stress on the breaker only and the SLF-test covers for this (case F in Chapter 2).
For the TRV envelope this phenomenon is therefore of minor importance.

The equipment in the substation are:
- 150kV cables,
- 300/150kV transformers and
- 150/50kV transformers

For transformer models especially the capacitance value is of importance.

In the discussion of reference /8/ O. Naef writes that he has acquired a good resemblance between measured and calculated TRVs when 40% of the total capacitance of a transformer winding or generator winding was used as value for a lumped representation.
As reactance the short circuit reactance for transformers and the (sub)transient reactance for generators is taken.

Diesendorf /48/ uses $L_T=0.75L_{air}$ and $C_T=0.4C_{winding}$ and claims satisfactory results.

This is supported by Parrott in /38/.
In this report Cigre Working Group 13-05 gives several equivalent circuits for transformers for transient recovery voltage studies.
These equivalent networks are especially useful for three-phase analysis with sequence networks.

In our calculation we will use the air gap reactance $L_T=L_{air}$ for transformers and the transient reactance $L_G=L'$ for generators.
By doing this, short circuit currents have the correct value.
An estimation of the capacitance is made based on measurements of the natural frequencies. Curves for the natural frequencies of the TRV oscillations are given in /36/.
The transformer capacitances can be calculated with $C_T=\omega/(4\pi^2 F_n^2.\omega L_T)$.

Resistive losses are neglected in the transformer model and this results in an amplitude factor slightly higher than practical situation.

For cables and lines the widely accepted EMTP constant parameter model is applied with distributed L and C and losses represented by a resistance R/2 in the middle and a resistance R/4 at both ends /51/.

4.5.3Analyses of TRVs in Cable Type Networks

Also for Cable Type Networks a differentiation between thermal and dielectric stresses is made.

The Short Cable Fault as the equivalent for the Short Line Fault for Overhead Lines will not be discussed since it is relatively harmless.

4.5.3.1.Dielectric stresses in Cable Type Networks

Dielectric stresses can be divided into two categories:

1. Dielectric stresses caused by Transient Recovery Voltages (TRVs). In particular the peak values are of importance for 3PCBs.
2. The dielectric stress as a result of power frequency Recovery Voltages (RVs) which after several tens of milliseconds after current interruption can cause a dielectric failure in the 3PCB /14,16,21/.

A 3PTM should therefore generate correct steady state AC recovery voltages with peak values and phase relations set by system parameters: voltage-level, phase-angle and frequency.

Substations in a Cable Type Network are in the majority of cases fed from a overhead line transmission network through powertransformers.
In CTNs therefore, the ratio of the short circuit current supplied by the transformers (I_{local}) and the total current (I_{tot}), i.e. I_{local}/I_{tot}, is higher than the values of around 30% found for Overhead Line Type Networks /3/ and can be close to 100% (see also section 4.4.2 on ROLTNs).

This is named the *bus-transformer-breaker-fault* /3/ or *transformer fed fault*, with a high amplitude factor γ of about 1.9.

Switching off short circuit currents which are fed through a transformer, could result in a higher RRRV than current IEC test duties define, even though cable characteristic impedances cause the dv/dt at interruption to be lower than the dv/dt in Overhead Line Type Networks.

The topology of these networks and substations is such that (almost) all short circuit power available in a substation is supplied by very large powertransformers (600 MVA and higher) and as a result the higher short circuit interrupting capability (Test Duties 3/4/5) could lead to a higher Rated Rise of Recovery Voltage /17,18,38/ than defined in IEC.

For this type of fault the inherent RRRV can be rather high /36,37/ with an initial slope S = 5.4 kV/μsec and initial peak factor σ = 1.5 but the dv/dt is commonly reduced to 3.5 kV/μsec for 80 to 90% of the maximum short circuit current /17/ in the Cable Type Networks the 3PCB has to interrupt. Note; compare current IEC Test Duty 4 values: S = 2 kV/μsec and σ = 1.3.

If other factors like the First Pole to Clear Factor do not differ too much from usual IEC values in (radial) Cable Type Networks, we can expect the Test Duty 3 (60%) and TD4/5 (100%) to have higher *TRV peak ratings* than currently used IEC values.

In order to verify these values and to come to more representative values for the dv/dt and initial peak factor σ we will analyse the TRVs in our benchmark substation (see section 4.5.1) connected to a Cable Type Network.

4.5.3.2.Thermal stresses for 3PCBs in Cable Type Networks

Besides the Rated Rise of Recovery Voltage 'RRRV' dv/dt, the di/dt influences the thermal stress even more, as we conclude from our discussion around Epa (chapter 2, section 2.4).

The di/dt for 3PCBs in Cable Type Networks will be different from the di/dt for open air 1PCBs operating in Overhead Line Type Networks. The large capacitance from the cable-sections and the GIS busbars distorts the current just before current zero by reducing the di/dt and eases the thermal stress for the arc by current commutation into the capacitance.

However, a 3PCB operating in either a Overhead Line or Cable Network will experience more or less the same thermal stress caused by the di/dt. Both environments provide the extra in parallel capacitance from short runs of cables and the GIS busbars.

Therefore our analysis for Meshed Overhead Line Type Networks (MOLTNs) on the influence of short runs of cables remains valid and our 3PTM applied to a 3PCB without the busbars or cable-sections, is more severe than the worst possible practical case of operating in an Overhead Line Type Network or operating in a Cable Type Network.

4.6 Transient Recovery Voltages

In this section the results of the numerical simulations with EMTP are given.

A single-phase analysis will be carried out first because this introduces all the major characteristics and is rather straightforward.

Both Cable Type Networks (CTNs) and Radial Overhead Line Type Networks (ROLTNs) are analysed.

After the single phase analysis, a three-phase calculation is performed to cope with the differences between single-phase and three-phase systems.

4.6.1The Benchmark system

Figure 4.4 shows a benchmark system having the relevant characteristics for TRV calculations in both Radial Overhead Line Type Networks (ROLTNs) and Cable Type Networks (CTNs).

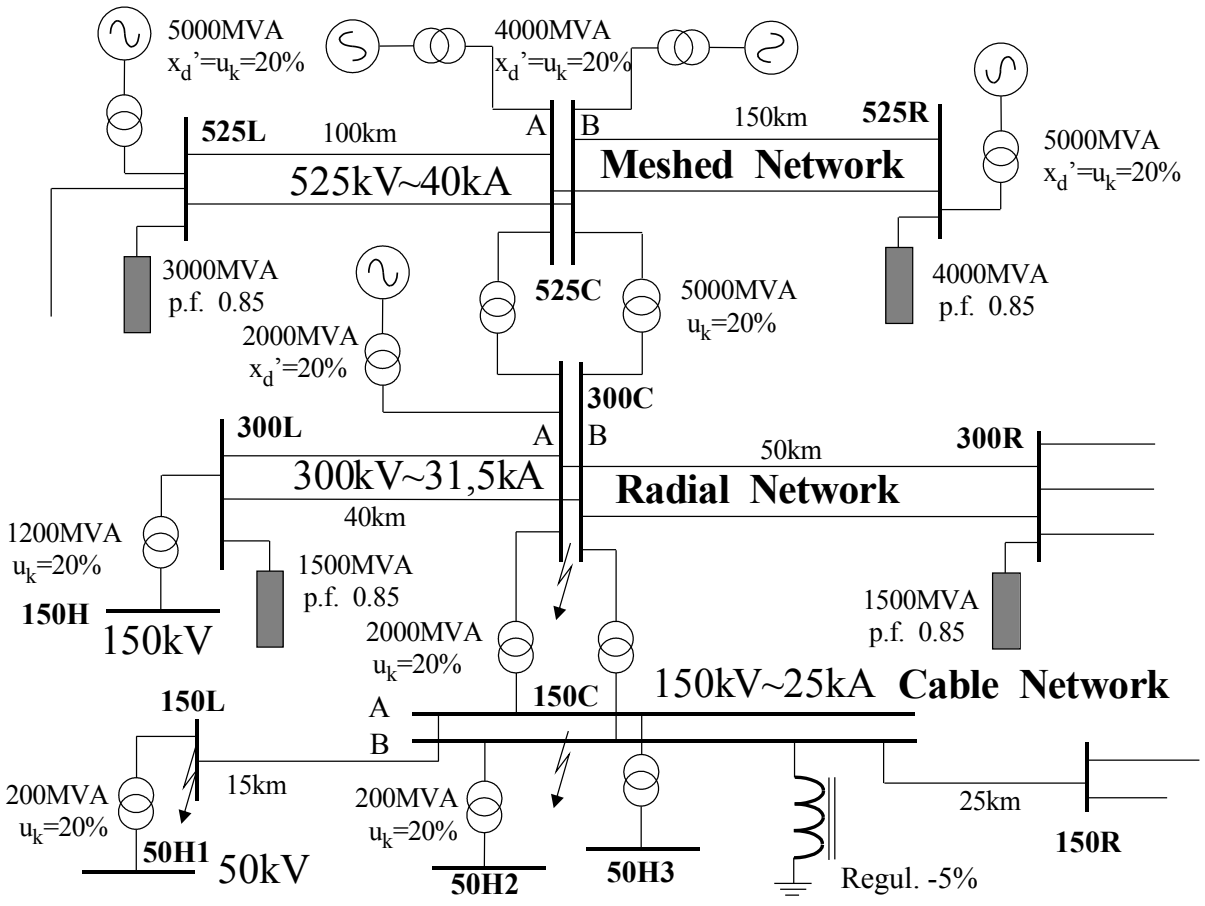

Fig. 4.4 One-line diagram of the Benchmark system

The system busses are; 525 kV (meshed): 525L, 525C and 525R
300 kV (radial): 300L, 300C and 300R
150 kV (radial): 150L, 150C, 150R and 150H
50 kV (distr.): 50H1, 50H2 and 50H3

The topology and other details of this network have been chosen such that the voltage levels and short circuit current levels give realistic values.

To investigate TRV characteristics in a ROLTN, a short circuit on bus 300C is made, and for TRV characteristics in a CTN short circuits are made on busbars 150C and 150L.

4.6.2Setting up the EMTP file with per unit elements

For Base Power we use Sb=1000MVA, resulting in:

- 525kV, Transmission Network, $Zb=525kV^2/1000MVA=275.6\ \Omega$
- 300kV, Transmission Network, $Zb=300kV^2/1000MVA=90.0\ \Omega$
- 150kV, Transmission Network, $Zb=150kV^2/1000MVA=22.5\ \Omega$
- 50kV, Distribution Network, $Zb=50Vk^2/1000MVA=2.5\ \Omega$
- 21kV, Generators, $Zb=21kV^2/1000MVA=0.441\ \Omega$

For the relevant component the parameters are listed below.

Because of the EMTP data format capacitances are in μ p.u (E-6 p.u.).

Generator: 4000MVA (=8x500), Xd'=0.2

$XG=0.2*(21kV^2/4000MVA)=0.02205\ \Omega$ --> Xg=0.05 p.u.

Gen Transformer: 4000MVA (8x500), uk=0.2, *F*n=4kHz

$XT=0.2*(525kV^2/4000MVA)=13.781\ \Omega$ --> Xt=0.0500 p.u.
$CT=\omega/(4\pi^2 F_n^2.\omega L)=\omega/(4\pi^2 F_n^2.Xt)$ --> $Xc^{-1}=\omega CT=3.125\ 10^3$ μ p.u.

Transformer 525/300kV: 5000MVA (5x1000), uk=0.2,
*F*n(525)=5kHz, *F*n(300)=9kHz

$XT=0.2*(525kV^2/5000MVA)=11.025\ \Omega$ --> Xt=0.04 p.u.
$CT=\omega/(4\pi^2 F_n^2.\omega L)=\omega/(4\pi^2 F_n^2.Xt)$ --> $Xc^{-1}(525)=\omega CT=2.50\ 10^3$ μ p.u.
--> $Xc^{-1}(300)=\omega CT=0.772\ 10^3$ μ p.u.

Transformer 150/50kV: 200MVA, uk=0.2, *F*n(150)=12kHz

$XT=0.2*(150kV^2/200MVA)=22.5\ \Omega$ --> Xt=1.000 p.u.
$CT=\omega/(4\pi^2 F_n^2.\omega L)=\omega/(4\pi^2 F_n^2.Xt)$ --> $Xc^{-1}(150)=\omega CT=17.361$ μ p.u.

Line 525kV: (Tower configuration of a 380kV line)

C=6.7 nF/km, L=2.44 mH/km, R=0.144 Ω/km, ℓ=100 km, so:
Zs=600 Ω --> Zs=2.177 p.u., $\upsilon=250.10^3$ km/sec, τ=0.4 msec
R=0.5225 10^{-3} p.u.

Load 300kV: 1500MVA, cosφ=0.85

$R=300^2/(0.85*1500)=70.6\ \Omega$ --> R=0.7843 p.u.
$XL=300^2/[(1-0.85^2)*1500]=113.9\ \Omega$ --> XL=1.2658 p.u.

Cables 150kV: solid core, lead armour/earth return

C=0.253 μF/km, L=1.58 mH/km, R=0.255 Ω/km, ℓ=15 km, so:
Zs=80 Ω --> Zs=3.555 p.u. $\upsilon=50.10^3$ km/sec, τ=0.3 msec
R=0.0113 p.u.

No Load 150kV: 200 km cables.

C=50.6 μF --> Xc^{-1}=0.01590 Ω --> $Xc^{-1}=0.358\ 10^6$ μ p.u.

Compensating reactor at 150kV bus:

Bus fault current Ik=25,8 kA --> Ireactor=(regulation/100)*Ik=1290 A
Regulation –5%
--> ωL=(Un/√3)/Ir=2.98 p.u.

4.6.3TRVs in Cable Type Networks

Five cases are calculated and the results of the calculations are analysed. For each case the IEC-60056 parameters which characterize the shape of the TRV, i.e. 4-parameter TRV, are derived.

For voltages of 100kV and above IEC prescribes 4-parameter TRVs, a two parameter representation seems adequate for transformer TRVs with high rates of rise and can be simulated with a single frequency circuit.

In the case of two parameter TRV's adapted parameters t_1' and U_1' are derived resulting in identical RRRVs compared with the 4-parameter method:

RRRV(IEC) = $U_1/t_1 = U_1'/ t_1'$.

4.6.3.1.Five cases of TRVs in Cable Type Networks.

i) As a first case we make a short circuit on the bus 150C - see the benchmark system of fig. 4.4 -, a configuration with two supply transformers, two outgoing ties, two unloaded step-down transformers and the compensating reactor, all directly connected to the substation.

This is situation a) as described in section 4.5.1, which can be seen as the reference fault situation and complies with IEC Test Duty 4 for Cable Type Networks (CTNs).

The transient-recovery voltage after current interruption is depicted in fig. 4.5;

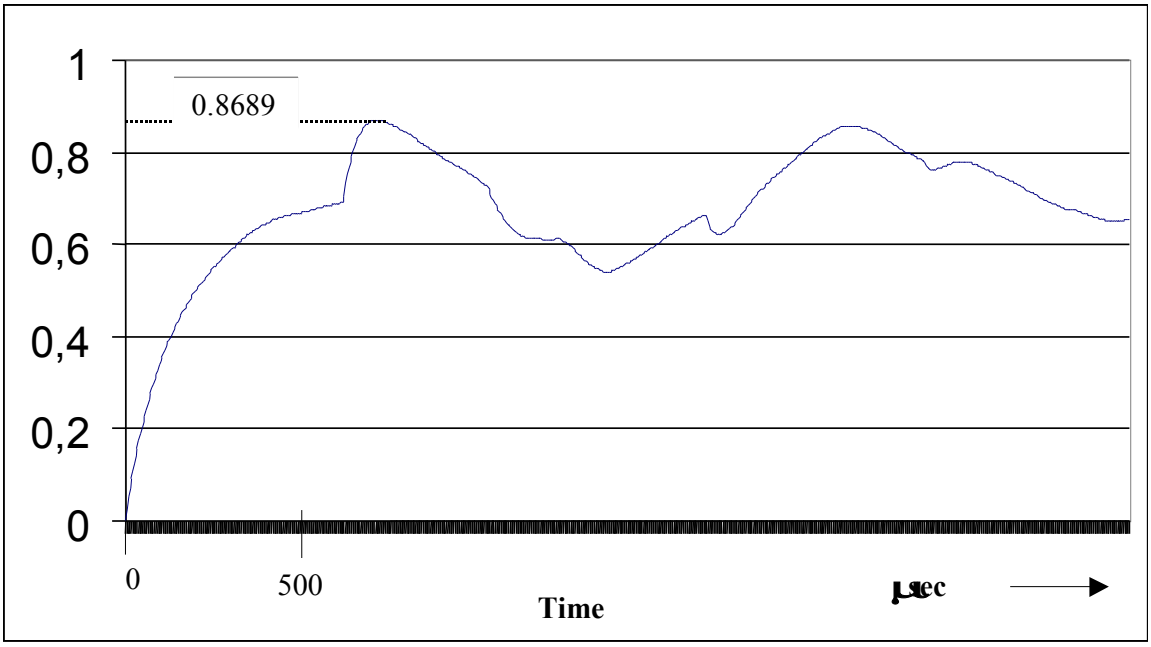

Fig. 4.5 TRV of a 100% fault (=TD4) in the 150kV network.

This is a typical example of a TRV built up of waves: reflections against a transformer-terminated end (150L) /24/ and reflections against a multiple line substation (150R).

The peak voltage U_c = 0.8689*150 = 130 kV (see fig. 4.5) and the 'driving voltage' ΔV = 0.8832*150 = 132 kV being the steady state voltage at the instant of interruption if no transient is present. The per unit numbers are the result of the EMTP simulations, 150 kV is the base voltage for the subnetwork under investigation.

Therefore the peak factor has the value:

$$\gamma = 130/132 = 0.99.$$

For this configuration the TRV is overdamped because of the influence of the cables and the lost transient energy which is dissipated in the 300kV supply Network.

We find a time t_1 = 63,4 µsec and a voltage U_1 = 0.424*150 = 63.6 kV, so the RRRV or S_1 is:

$$S_1 = U_1/t_1 = 1.00 \text{ kV/µs}.$$

This is within the expected range from 0.5 to 2 kV/µs.

As can be seen in Figure 4.5 this TRV has almost no delay time, even if we zoom into a much smaller time scale (µsec).

The first-peak factor of the TRV is: $\sigma = U_1/\Delta V = 0.424/0.8832 = 0.48$.

Although normalized TRV ratings like amplitude factor and first-peak factor are exact when we use the 'driving voltage' ΔV because local voltage level and phase shifts are taken into account; the figures are not the same as listed in IEC.

In the IEC the nominal voltage level for normalizing is used, $(\sqrt{2}/\sqrt{3})*U_n$.

If we use this definition we come to:

$\gamma_n = 0.8689/0.8165 = 1.06$ and $\sigma_n = 0.424/0.817 = 0.52$

ii) As a next case the 'alternate' maximum short circuit current in situation b) as defined in section 4.5.1 which also concurs with Test Duty 4, having two supply transformers connected and only one tie behind the breaker at which spot a Breaker Terminal Fault (BTF) occurs, being equivalent to a bus fault.

This is the fault situation where the current stress is comparable with the reference situation (100% of rated short circuit current) but, because of the absence of cables, the TRV is largely determined by the characteristics of the supplying transformers.

After a network calculation we find;

Peak voltage $U_c = 1.1402*150 = 171$ kV and a 'driving voltage' $\Delta V = 0.8994*150 = 135$ kV. The peak factor becomes:

$\gamma = 171/135 = 1.27$ and $\gamma_n = 1.1402/0.8165 = 1.40$

This is still a rather low value, caused by the fact that only a reduced percentage of the driving voltage is across the transformer, and thus reducing the effective amplitude factor /40/. The peak factor is also reduced by the damping to the 300kV side.

We find a time $t_1' = 18{,}8$ μsec and a voltage $U_1' = 0.859*150 = 129$ kV, so the RRRV or S_1 is:

$S_1 = U_1'/t_1' = 6.85$ kV/μs.

This is a typical value for a transformer-through-fault RRRV and fits rather neatly with what is published in /56/.

The delay time for this TRV is $t_d = 1.7$ μs and this is rather small.

The first peak factor is $\sigma = 1.115/0.8994 = 1.24$ [and normalised for $(\sqrt{2}/\sqrt{3})*U_n$: $\sigma_n = 1.115/0.817 = 1.37$], which again is lower than expected due to the reduced amplitude factor and damping at the 300kV side.

iii) If we calculate the maximum short circuit current again as in case ii) [see situation b) in section 4.5.1.], but have the two step-down transformers (150/50kV) and a reactor connected as well, we have a check on simulation ii, to see whether the step-down transformers change the TRV significantly.

We find, after calculation;

A peak voltage $U_c = 0.9806*150 = 147$ kV and a 'driving voltage' $\Delta V = 0.8866*150 = 133$ kV. Therefore the peak factor is:

$\gamma = 147/133 = 1.11$ and normalised $\gamma_n = 0.9806/0.8165 = 1.20$

This is an even lower value compared with case ii), and this is caused by the charging of the capacitances at the 50kV side and the damping at the 300kV side.

We find a time t_1' = 19,5 μsec and a voltage U_1' = 0.800*150 = 120 kV, so the RRRV or S_1 is:

$S_1 = U_1'/t_1'$ = 6.15 kV/μs.

And this is within the expected range.

The delay time t_d = 2.3 μs and

the first-peak factor is:

σ = 0.9527/0.8866 = 1.08 and σ_n = 0.9527/0.8165 = 1.17

Although a bus capacitance was not taken into account, this would not alter the TRV significantly, since this capacitance is rather small and of no influence on the TRV, as can be read in /57/.

What we do not find is a significant increase in peak voltages as a result of oscillations. This is caused by the fact that the frequencies involved are very low (large capacitances) compared to the transient recovery voltages and that their amplitude is rather small.

iv) Next we will investigate the situation for the 150kV bus fed by one transformer (comparable with IEC test duty 3) and a short circuit just behind the breaker of the tie which is still connected to the bus.

This simulation is comparable with situation c) as defined in section 4.5.1.

In this case we can expect a TRV wave-form comparable with simulation ii) and iii) having a peak and a dv/dt that are even higher.

The transient recovery voltage, after current interruption is depicted in fig. 4.6;

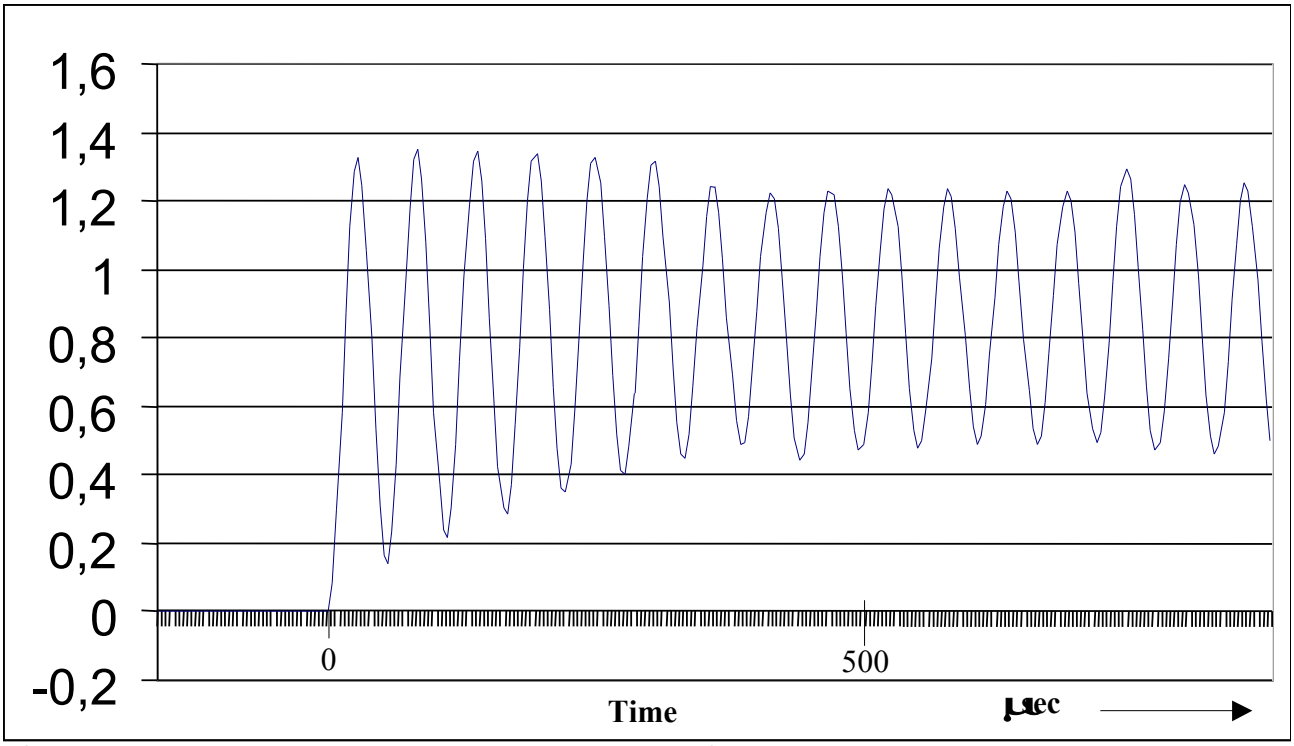

Fig. 4.6 TRV of a 50-60% fault (IEC TD3) in the 150kV network.

This is a classical TRV wave form of a transformer fault /9/ and comparable with simulation ii) and iii).

The peak voltage U_c = 1.3501*150 = 203 kV and the 'driving voltage' ΔV = 0.9004*150 = 135 kV. And the peak factors result in:

γ = 203/135 = 1.50 and γ_n = 1.3501/0.8165 = 1.65

This is a slightly higher value than in the case of the TRV for two supply transformers, since now a greater part of the supply voltage is across the transformer, thereby reducing the effective TRV driving voltage although the damping at the 300kV side has less influence.

We measure a time t_1' = 17,7 µsec and a voltage U_1' = 1.00*150 = 150 kV, so the RRRV S_1 is:

$S_1 = U_1'/t_1'$ = 8.47 kV/µs.

Due to the higher effective amplitude factor this value is higher than in the situation of two supply transformers.

The delay time t_d = 2.4 µs

The first-peak factor becomes:

σ = 1.3301/0.9004 = 1.48 and σ_n = 1.3301/0.8165 = 1.63

v) As a last case we will investigate a fault on the 150L bus. This is comparable with Test Duty 1 and 2, being situation d) as defined in section 4.5.1., when identical breakers are installed in substations 150C and 150L. We find;

a peak voltage U_c = 1.1022*150 = 165.3 kV and a 'driving voltage' ΔV = 0.8397*150 = 126 kV. Therefore the peak factor is:

γ = 165.3/125.9 = 1.31 and γ_n = 1.1022/0.8165 = 1.35

This is a higher value than in the case of the TRV for bus 150C, since the driving voltage is boosted by the ferranti-effect of the capacitance of the cable in the short circuit path.

Furthermore we measure for t_1 = 345 μsec and U_1 = 0.956*150 = 143 kV, so the RRRV or S_1 is:

$S_1 = U_1/t_1$ = 0.42 kV/μs.

As expected, this is a much lower value than IEC gives.

Again there is no delay time.

The first-peak factor:

σ = 0.9774/0.8397 = 1.16 and σ_n = 0.9774/0.8165 = 1.12

4.6.3.2.Summary on TRVs in a Cable Type Network

If we table the parameters found for the single phase TRV simulations in a Cable Type Network (CTN) as shown in the benchmark system of fig. 4.4, we get:

Case	Description	S_1 kV/μs	γ_n	σ_n
i	Reference fault TD4 in CTN, all components connected	1.00	1.06	0.52
ii	Alternate fault (~TD4), two supply transformers	6.85	1.40	1.37
iii	Alternate fault (~TD4), all transformers, reactor	6.15	1.20	1.17
iv	Alternate fault (~TD3), one supply transformer	8.47	1.65	1.63
v	Reference fault TD1&2 in CTN	0.42	1.35	1.20

Table 4.8 Results of TRV simulations in a CTN

As expected, we find much higher values for the RRRV when no cables are connected at the bus in comparison with the reference fault situation or the IEC.

The first peak factor σ_n was in some cases found to be a bit higher than IEC for this voltage level: 1.3.

Noteworthy is the fact that for TRVs with cables connected to the bus, we did not find any significant delay times and for transformer TRVs the delay times were still rather short.

We did not find an increased peak factor γ since the reduced amplitude factor apparently plays an important role.
Possible oscillatory situations were found in some cases (e.g. fig 4.6) but apparently not influencing the peak factor in a significant way.

This is different from what Bonfanti et al. /57/ found. They found that when a cable is added to a transformer-fed fault, the TRV peak is likely to increase.

4.6.4TRVs in Radial Overhead Line Type Networks

To verify findings in literature (table 4.6 & 4.7) with calculations for Radial Overhead Line Type Network TRVs we will now analyse the 300kV part of our benchmark system.

4.6.4.1.Four cases of TRVs in a Radial Overhead Line Type Network

i) As a first case to be calculated we will simulate a reference short circuit on bus 300C with all components connected. That is a fault situation comparable with TD4 in a ROLTN.

We find;

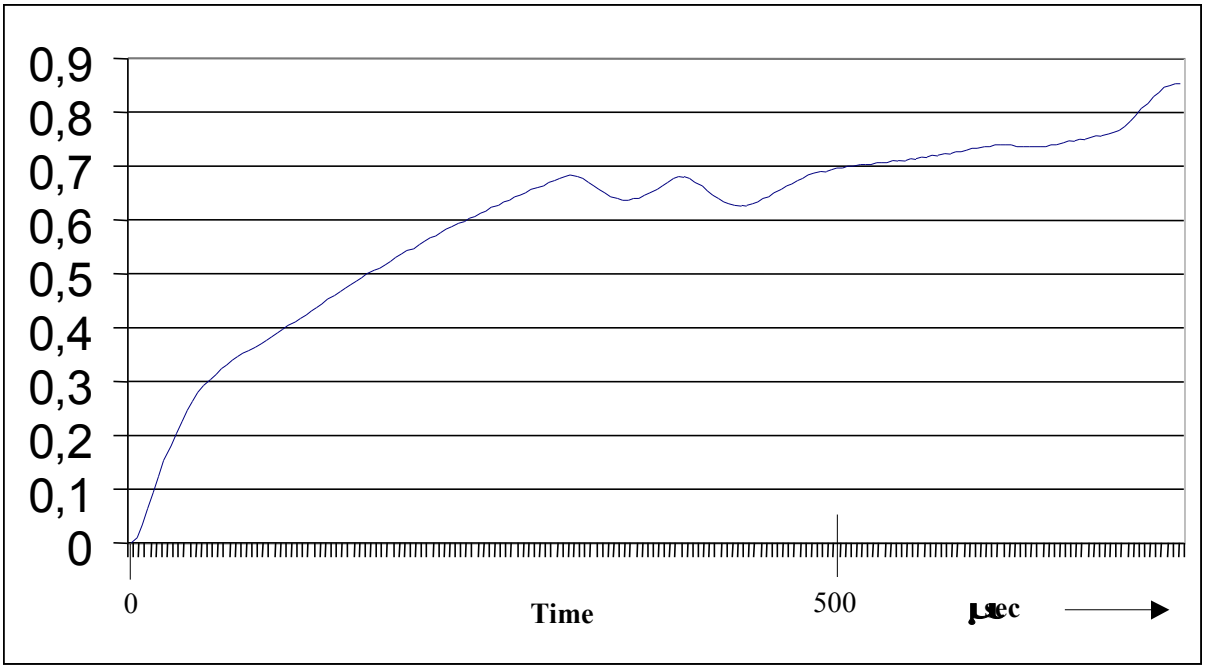

Fig. 4.7 TRV of a 100% fault (=TD4) in 300kV network.

Again this is a typical TRV waveform for Overhead Line Type Networks /24/.

The peak voltage U_c = 0.8544*300 = 256 kV and the 'driving voltage' ΔV = 0.8970*300 = 269 kV. Therefore the peak factors come at:

γ = 256/269 = 0.952 and γ_n = 0.8544/0.8165 = 1.046

This is an overdamped response caused by reflections on the overhead lines and the damping from the 525kV supply side.

We measure a time t_1 = 98 µsec and a voltage U_1 = 0.582*300 = 175 kV, so the RRRV S_1 is:

$S_1 = U_1/t_1$ = 1.79 kV/µs.

This is within the familiar range of 1.0 to 2.0 kV/μs, but it is much lower than will occur when no lines are connected to the bus (as will become clear later).

The transformer capacitances are clearly visible in the delay time:

$t_d \approx 3$ μs

This is in line with the IEC value for similar voltage levels: $t_d = 2$ μs.

The first-peak factor $\sigma = 0.582/0.8970 = 0.65$ ($\sigma_n = 0.71$). This is higher than found in Cable Type Networks since the damping by characteristic impedances is less pronounced.

ii) As a next case the breaker interrupts an alternate 100% short circuit on the 300C bus (~ TD4), but with only two 5000MVA supply transformer banks, the 2000MVA power plant and one feeder behind the breaker where the fault occurs, connected to the bus (so no lines attached). The calculation results in;

a peak voltage $U_c = 1.219*300 = 366$ kV and a 'driving voltage' $\Delta V = 0.9745*300 = 292$ kV. The peak factors are:

$\gamma = 366/292 = 1.25$ and $\gamma_n = 1.219/0.8165 = 1.50$

This is a value influenced by the reduced 'driving' voltage /40/ and damping of the 525kV supply side.

Furthermore we measure a time $t_1' = 47.3$ μsec and a voltage $U_1' = 0.851*300 = 255$ kV, so the RRRV S_1 is:

$S_1 = U_1'/t_1' = 5.40$ kV/μs.

This is typical for a transformer fed fault and higher than the averaged values of ~4 kV/μs found in literature.

Because of the transformer capacitance the delay time is clearly visible:

$t_d \approx 7$ μs

The first-peak factors are $\sigma = 0.8634/.9745 = 0.89$ and $\sigma_n = 0.86$.

iii) This case is as case ii), but the two step-down transformers are connected to the bus as well. The calculation results in;

a peak voltage $U_c = 1.1240*300 = 337$ kV and a 'driving voltage' $\Delta V = 0.9718*300 = 292$ kV. Therefore the peak factors are:

$\gamma = 337/292 = 1.15$ and $\gamma_n = 1.1240/0.8165 = 1.38$

This value is influenced by the reduced 'driving' voltage and damping from both the 525kV supply side and the 150kV side.

We measure a time t_1' = 29.4 μsec and a voltage U_1' = 0.640*300 = 192 kV, so the RRRV S_1 is:

$$S_1 = U_1'/t_1' = 6.53 \text{ kV/}\mu\text{s}.$$

Because of the two additional transformers this value is higher than in case ii).

Because of the transformer capacitance the delay line is considerable:

$$t_d \approx 7 \ \mu\text{s}$$

The first-peak factors are σ = 0.652/0.972 = 0.67 and σ_n = 0.80.

iv) As a final single phase calculation we will analyse a bus fault fed by only one transformer, no other components connected to the bus, a situation comparable with TD3. After calculation we find;

a peak voltage U_c = 1.2942*300 = 388 kV and a 'driving voltage' ΔV = 0.9437*300 = 283 kV. The peak factors are:

$$\gamma = 388/283 = 1.37 \quad \text{and} \quad \gamma_n = 1.2942/0.8165 = 1.59$$

Even this value is influenced by a reduced 'driving' voltage and damping at the 525kV supply side.

We measure a time t_1' = 50,4 μsec and a voltage U_1' = 1.150*300 = 345 kV, so the RRRV S_1 is:

$$S_1 = U_1'/t_1' = 6.85 \text{ kV/}\mu\text{s}.$$

This is a rather high value as can be expected.

Because of the transformer capacitance the delay line is considerable:

$$t_d \approx 7 \ \mu\text{s}$$

The first-peak factors are σ = 1.159/0.9437 = 1.23 and σ_n = 1.42.

4.6.4.2.Summary on TRVs in a Radial Overhead Line Type Network

If we table the results of the ROLTN simulations we get:

Case	Description	S_1 kV/μs	γ_n	σ_n
i	Reference fault TD4 in ROLTN, all connected	1.79	1.05	0.71
ii	Alternate fault (~TD4), full supply, no lines	5.40	1.49	0.86
iii	Alternate fault (~TD4), all transformers	6.53	1.38	0.80
iv	Alternate fault (~TD3), one supply transformer	6.85	1.59	1.42

Table 4.9 Results of TRV simulations in a ROLTN

As expected we have found an increased Rated Rise of Recovery Voltage (RRRV), even above values found in literature. An explanation could be that the damping, as reported in literature studies, is more dominant.

The higher RRRVs come with an increased delay time t_d, which is understandable because there is a resemblance between a Transformer Transient Recovery Voltage (TRF TRV) and a '1-cos' TRV.

4.6.5Which TRV is the most severe for the circuit breaker ?

Before tabling our mostly dielectric results, from the literature and the simulation studies, it is interesting to know which is *thermally* more severe:

a) An overdamped 4-parameter TRV according to IEC with a $t_d \approx 2\mu s$ and a RRRV ≈ 2 kV/μs and a peak factor of 1.4 or a transformer TRV ('1-cos' wave) with a longer delay time or
b) The TRV according to IEC or a slower TRV (RRRV 1 kV/μs and peak factor of 1.0) but with almost no delay or
c) Any of the above three Breaker Terminal Fault (BTF) TRVs or a Short Line Fault (SLF) TRV oscillation.

To get insight into a) we will analyse a TD4 test for a 245kV/40kA (60Hz) SF6 breaker in a direct circuit where the overdamped TRV oscillates in a conventional TRV network and the transformer TRV comes from an 300:300kV transformer in series, this produces a clear '1-cos' oscillation with the same peak as the overdamped TRV (364kV).

The transformers are taken as five 750MVA units with a short circuit ratio of u_k=0.2, and from /36/ the oscillation frequency can be found:
*F*n = 10 kHz.

As circuit breaker model we will use an Urbanek model with parameters for an SF6 circuit breaker. The results of the calculation are;

	IEC 4par TRV (SF6)	TRF TRV (SF6)
Epa (Ws)	0.00924022	0.0175246

Table 4.10. Thermal severity of 4par TRV and TRF TRV

From the results we conclude that the Transformer TRV (TRF TRV), with a RRRV = 300kV/36μs = 8.3 kV/μs, is more severe than the 'standard' TRV with a relatively low RRRV = 150kV/70μs = 2.1 kV/μs.

As discussed in the Chapter on Epa the thermal severity depends on the duration and amplitude of the post-arc current.

Even if we change the parameters from the Urbanek model such that we reduce the post arc current to lower values we get the same results, and the Transformer TRV remains more severe than the IEC defined standard TRV.

To get insight into b) we will again analyse a TD4 test for a 245kV/40kA (60Hz) SF6 breaker in a direct circuit where the standard TRV is generated by a conventional TRV network and the TRV without delay is generated by a tuned TRV-Network. The latter produces a clear R-L response /40/ with a RRRV of 1.00 kV/μs, the peak is lower than the standard TRV but this has no consequence for the thermal stress. The results of the calculations are in table 4.11;

	IEC 4par TRV	TRV without delay
Epa (Ws)	0.00924022	0.01483455

Table 4.11 Thermal severity of 4par TRV and TRV without delay

The 'weak' TRV with the low RRRV and without delay time is more severe than the IEC 4-parameter IEC TRV.

To get insight into c) we will analyse our TD4 direct test circuit with its standard TRV to test the 245kV/40kA/60Hz SF6 circuit breaker but add a piece of short line (distributed line model) with the standard IEC characteristic impedance of 450 Ω.
If the circuit breaker fails a certain range of line lengths (ℓ), it is clear that the SLF TRV is more severe in the thermal region than in any of the Breaker Terminal Fault (BTF) situations. We find;

	$\ell \leq$ 0.05 km	$\ell \geq$ 3.75 km
Epa-max	0.08167042 Ws	0.0367869 Ws

Table 4.12 Thermal severity of a SLF TRV

Between 0.05 and 3.75 km line length the breaker model did not interrupt.

So we can conclude that the SLF TRV is definitely more severe than any of the BTF situations.

4.6.6Three-phase verification for the single-phase TRV computations

For the sake of computational ease the above analyses have been done single-phase. The main characteristics of TRVs (RRRV, first peak, and amplitude factor) are easily found with single-phase analyses.

To prove that the single-phase results can be used for the majority of three-phase networks and to show some typically three-phase characteristics (Pole to Clear Factors, across-phase influences) we will now analyse the benchmark system of fig. 4.4 as a complete three-phase network.

4.6.6.1.Setting up the three-phase network

The practical difference between single-phase networks and three-phase networks is that the mutual influences between phases give extra paths for electro-magnetic energy exchanges.

These paths are created by the capacitive and inductive coupling of lines and cables and through transformers.
Another path is through the neutral impedance, which is a common factor for the three phases.

So, when setting up our three-phase (benchmark) network we have to carefully model lines, cables and transformers such that the couplings are represented.
The network must also allow for the different earthing practices, effectively earthed, reactance earthed and even an isolated neutral.

Lines/cables.

To model lines and cables the Constant Parameter model for continuously transposed lines implemented in the EMTP is used.

This model is an approximation because ‘continuously transposed’ lines are an ideal situation and not applicable to buried cables, but it allows for realistic cross influences; the difference between the more realistic untransposed modelling and transposed modelling is of no great consequence for the more general TRV characteristics.

The model uses so-called modal parameters, which are calculated, by using the ‘AUX-routines’ of the EMTP.

For the 100km 525kV ‘Double-Circuit’ between 525L and 525CA/B the modal parameters are:

```
C   BUS1  BUS2 RBUS1 RBUS2 RESIS  ZS     V   LNGTH L P P                      O
C |    *|    *|    *|    *|    *|    *|    *|    *|*|*|*----------------------*
C TRANSMISSION DOUBLE-LINE BUS 525L TO 525CA&525CB
-1 525LA525CAA            .2377 2034. 2.90E5  100. 1
-2 525LB525CAB            .1257 589.7 2.95E5  100. 1
-3 525LC525CAC            .1257 426.9 2.92E5  100. 1
-4 525LA525CBA
-5 525LB525CBB
-6 525LC525CBC
```

Note that the resistance and characteristic impedance are non-normalized (normalized = per unit method) since this creates problems when representing transformers.

Transformers.

Transformers are modeled by modified π-sections, so called: R-L Branches. This modelling includes magnetic cross influences, copper losses and no-load (magnetizing) currents, but it does not include capacitive coupling.

Since the EMTP uses the Nodal Admittance method and works in admittances, it calculates the inverse of the impedance matrices (Z) to get the admittance matrices (Y). This causes problems when we work with per unit representations in R-L Branches for transformers because the determinant of the normalized impedance matrix (calculated with Cramer's rule) is zero. In our three-phase network we use the normal representation with non-normalized impedance and the correct voltages and currents in the networks.

For a 1200MVA 300/150kV transformer (at bus '300L') the transformer parameters are:

```
C   BUS1  BUS2 RBUS1 RBUS2  RKM        LKM   RKM+1     LKM+1   RKM+2     LKM+2
C |    *|    *|    *|    *|    *|          *|    *|          *|    *|          *
C LOAD TRANSFORMER 300/150KV T300L
51 300LA 300LN            .03750 31969.05293
52 300LB 300LN                 -15972.58999.03750 31969.05293
53 300LC 300LN                 -15972.58999      -15972.58999.03750 31969.05293
54 150HA 150HN                  15972.58999       -7986.29500       -7986.29500
                         .00937  7992.26323
55 150HB 150HN                  -7986.29500       15972.58999       -7986.29500
                                -3993.14750.00937  7992.26323
56 150HC 150HN                  -7986.29500       -7986.29500       15972.58999
                                -3993.14750       -3993.14750.00937  7992.26323
```

This 'Lower triangular R-L matrix' was made with the use of a routine, which constructs this matrix from normal input data like Power, Voltage, Nominal and Magnetizing Currents, Short Circuit Percentage etc. The routine was written for this purpose by the Power Systems Laboratory of Delft University /52/.

Capacitive influences, like winding capacitances and the capacitive coupling between primary windings and secondary windings, can be added as lumped capacitances.

The capacitive influences are already accounted for when the natural frequency capacitances, added to the terminals, are derived from measurements /36/.
In our single and three-phase analysis the lumped capacitances were added.

Neutral impedances.

Neutral impedances can be added as a resistance, inductance and/or capacitance, at the neutral nodes of the transformers, like the nodes '300LN' and '150HN' (see transformer example).

4.6.6.2.Results of three-phase TRV analyses.

First we will analyse effectively earthed networks /54/; this means that on the voltage level of interest all transformer neutrals are solidly earthed resulting in the total $X_0/X_1 < 3$ on that voltage level.

4.6.6.2.1.Radial Overhead Line Type Networks.

Similar as for the single-phase analyses a short circuit (3LG) is made on bus 300C with all components connected including lines. The calculation results are plotted in fig. 4.8;

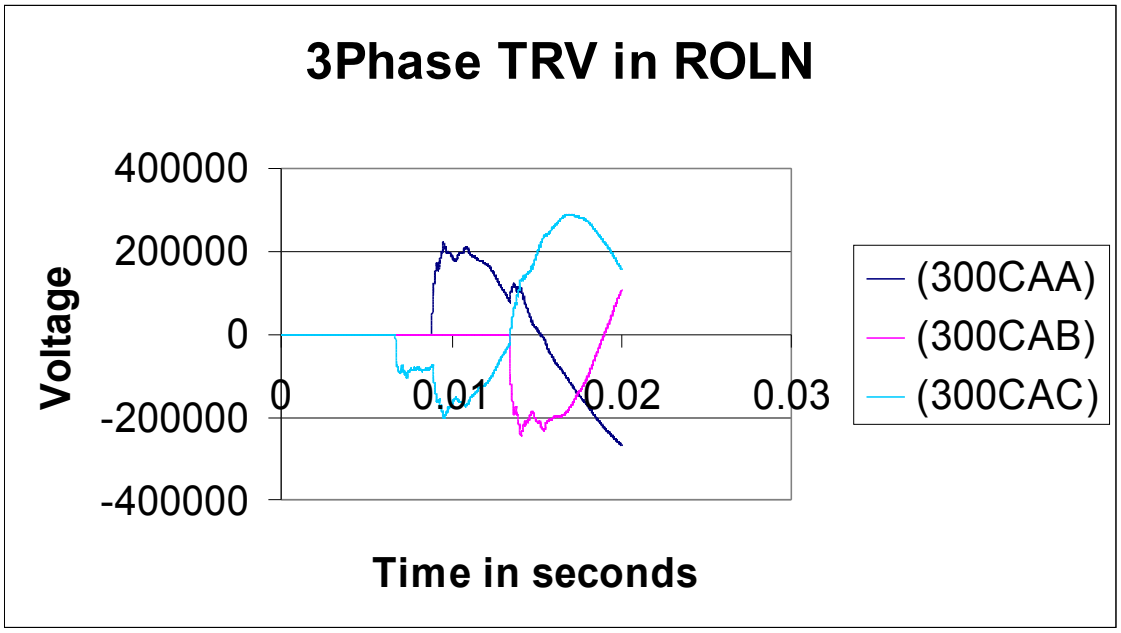

Fig. 4.8 TRVs of a 100% fault (=TD4) in three-phase 300kV network.

The phase sequence is C, A and B.

For the first pole to clear (pole C) we notice that the TRV has two distinct parts, i.e. a first part when the current in the phase itself is interrupted and a second part, with a much higher peak voltage, when the current in the second phase (A) is interrupted.

That the TRV is composed from two parts can be explained by means of sequence networks.

If we approximate the steady state voltage of the first pole to clear by means of a double line to ground fault (2LG) with fault impedance Z_f, and assume no load-current to flow in the fully symmetrical prefault situation the value of the voltage at the Fault location (bus k) being V_f, we can write for the sequence currents of the healthy phase 'a' /53/:

$$I_{fa}^{(1)} = \frac{V_f}{\left[Z_{kk}^{(1)} + \left(\frac{Z_{kk}^{(2)} (Z_{kk}^{(0)} + 3Z_f)}{Z_{kk}^{(2)} + Z_{kk}^{(0)} + 3Z_f} \right) \right]}$$

$$I_{fa}^{(2)} = -I_{fa}^{(1)} \frac{Z_{kk}^{(0)} + 3Z_f}{Z_{kk}^{(2)} + Z_{kk}^{(0)} + 3Z_f}$$

$$I_{fa}^{(0)} = -I_{fa}^{(1)} \frac{Z_{kk}^{(2)}}{Z_{kk}^{(2)} + Z_{kk}^{(0)} + 3Z_f}$$

And the sequence voltages of phase 'a' on bus j in the case of a 2LG-Fault at bus k are:

$$V_{ja}^{(0)} = -Z_{jk}^{(0)} * I_{fa}^{(0)}$$

$$V_{ja}^{(1)} = V_{pf} - Z_{jk}^{(1)} * I_{fa}^{(1)}$$

$$V_{ja}^{(2)} = -Z_{jk}^{(2)} * I_{fa}^{(2)}$$

In these formulae $Z_{jk}^{(i)}$ are the sequence impedances (i=0,1,2) 'seen' from bus j with a 2LG-Fault at bus k and V_{pf} is the actual prefault voltage at bus j (V_f at bus k).

These equations make clear that the ratio of zero sequence impedance / positive sequence impedance is rather influential.

We assume Ynyn transformers for every voltage level with solidly earthed neutrals at 525kV and 300kV but reactance earthed neutrals X_n = 12.5 Ω at 150kV and X_n = 6.25 Ω at 50kV.

The neutral impedances in particular, but also the fault impedance Z_f influence the ratio zero / positive sequence impedance $[Z^{(0)}/Z^{(1)}]$ and cause the 'healthy' phase voltage to differ from the single-phase case or the completely uncoupled situation.

We find $V_{ka} \approx 93$ kV in the actual network, which is rather different from the prefault voltage level.

If we calculate the amplitude factors per phase from the digital data using the expression:

$$\gamma = (\text{TRV-peak})/(\text{peak steady state voltage of that configuration})$$

we get, $\gamma_C = 103345/93213 = 1.109$,
$\gamma_A = 222201/233208 = 0.953$,
$\gamma_B = 243866/262423 = 0.929$

This way of calculating overlooks the non-ideal phase-shift between current and voltage (being not exactly 90° inductive), but that is of minor importance.

It is the last pole to clear that gives the highest absolute peak values (243 kV > 222 kV > 103 kV).

For reasons of symmetry it is the last pole to clear (pole B) that resembles the single-phase analysis most, because the unbalance in electro-magnetic energy released cannot find a path through other phases as easily as is the case for the first and second pole to clear where the energy can balance itself through mutual coupling and through the paths created by the other circuit breaker poles that are still conducting.

In fig. 4.9 the transient recovery voltages across pole B is enlarged:

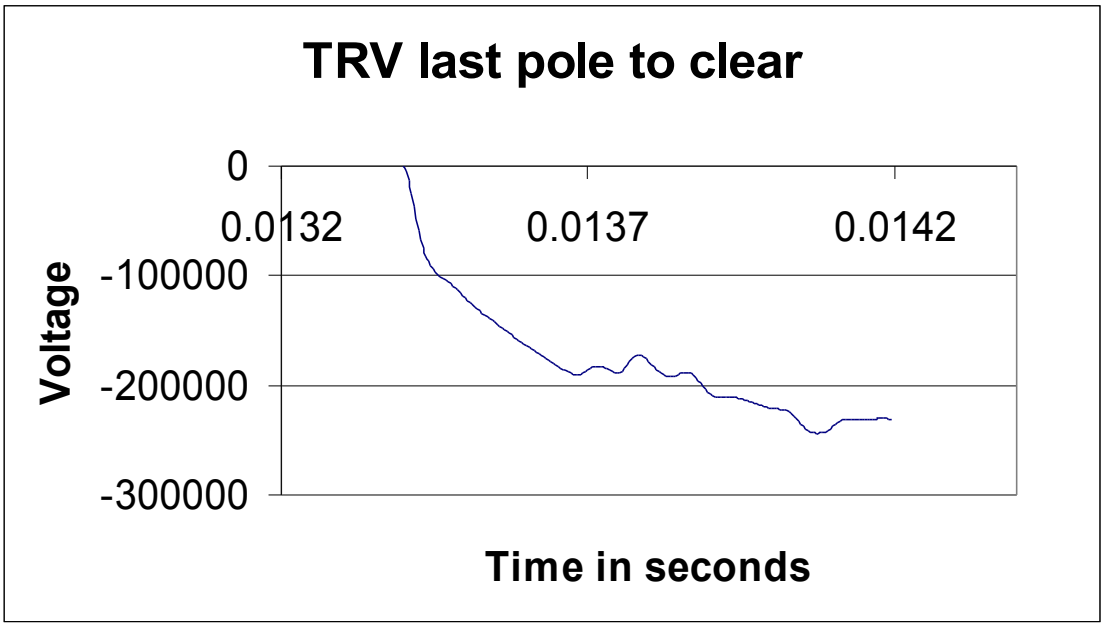

Fig. 4.9 Enlarged view of TRV across pole B.

If we compare this TRV with Figure 4.7 we see a rather similar plot.

The related parameters S_1 and t_d are: $S_1 = 60/24 = 2.5$ kV/μs, $t_d \approx 4$ μs.

The amplitude factor γ_B, the rated rise of recovery voltage S_1 and the delay time t_d do not differ much from the single-phase analysis, even though the RRRV is also influenced by the pole to clear factor and type of fault /59/.

As a next example an alternate full short circuit on the 300C bus is interrupted, comparable with IEC TD4, but only with the two 5000MVA supply transformer banks, the 2000MVA power plant and one feeder behind the breaker where the fault occurs connected to the bus. There are no lines connected.

Fig. 4.10 shows the TRV across the last pole to clear (pole B);

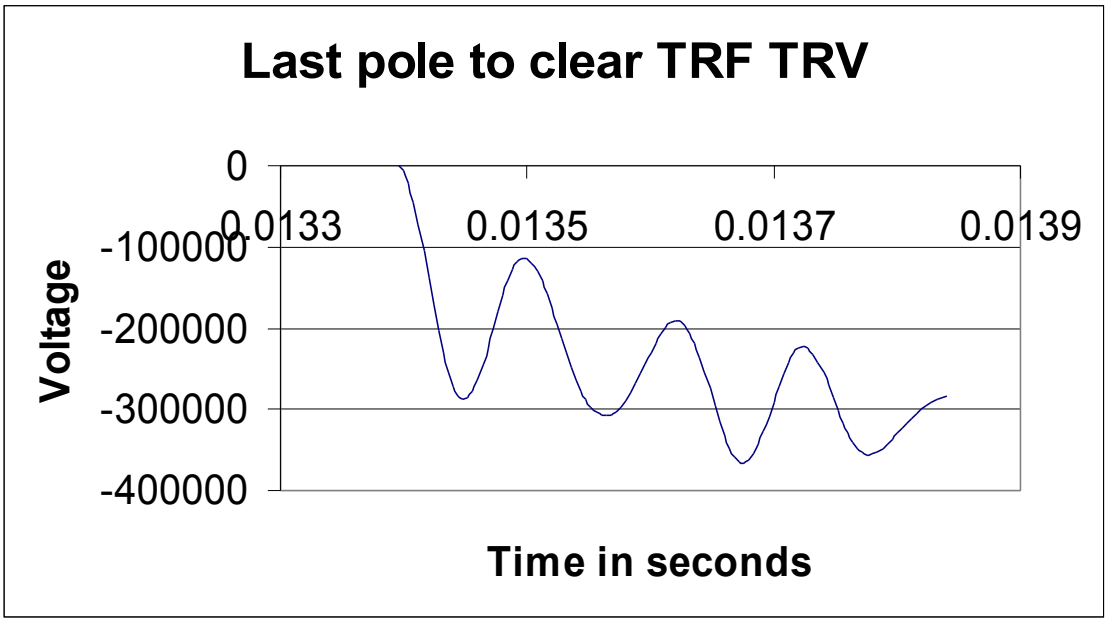

Fig. 4.10 Last pole to clear TRV of alternate 100% fault (~TD4).

The measured TRV parameters are:

S_1 = 202.4/32 = 6.3 kV/μs
σ = 288.6/290 = 1.00 ; t_1 = 52 μsec
γ = 377.1/290 = 1.30 ; t_c = 600 μsec
t_d = 5 μsec

If we compare these values with the measured values of the single-phase analysis we see that there are differences, for the first-peak value and the RRRV.
The differences are such that the three-phase values can be regarded even more 'severe'. The general overall behaviour is, however, more or less the same.

4.6.6.2.2.Pole to Clear Factors.

Now we will analyse networks where the transformer neutrals are reactance-earthed or even isolated /54/.

4.6.6.2.3.Cable Type Networks.

We will use the CTN-part at 150 kV of our benchmark system for a reactance-earthed analysis.

Therefore in this case at every transformer neutral is earthed over a reactance with an ohm value of 12.5 Ω at power frequency.

In cable networks in practice the neutral will either be isolated or earthed over an neutral impedance large enough to limit the return current through the cable-screens to a value low enough to be sustained for the maximum relay detection times.

As a first case we will make a short circuit on bus 150C with all other components connected, that is with two supply transformers, two outgoing ties, two unloaded step-down transformers and the compensating reactor. Fig. 4.11 shows the TRV-plots;

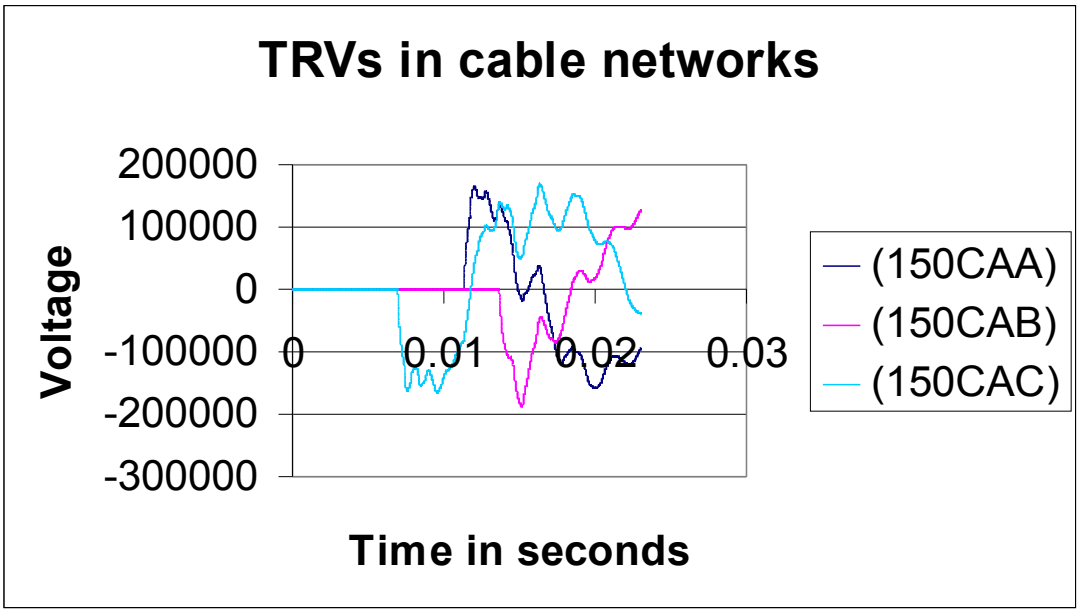

Fig. 4.11 TRVs of a 100% fault (=TD4) in three-phase 150kV network.

From fig. 4.11 we see that the TRVs are much more prolonged as compared with the overhead line cases since damping is low because of short cables and no loads connected.

The first pole to clear factor can be calculated if we have the steady state voltage on phase C in the situation with phase A and B still faulty and compare this with the voltage on phase C if everything is healthy:

$$FPCF = 178175/133970 = 1.33$$

The FPCF value can be explained with the formula given in /20/ as was referred to earlier.

In this case the value of $k = X_0/X_1$ is found to be $k = 4$, which clearly indicates that on this voltage level the system is reactance-earthed.

If we approximate the network 'seen' by the fault by two 300/150kV transformers of 2000MVA in parallel we get:

$$k = X_0/X_1 = 6.25/1.125 = 5.56$$

which results in a First Pole to Clear Factor:

$$FPCF = \frac{3k}{1+ 2k} = 1.38$$

This is rather similar to the value we found in our calculations, which includes the whole network 'seen' from the fault, i.e. transformers, cables, reactor and neutral impedances.

Another way to find the actual ratio k would be to perform short circuit simulations with a three-phase fault and repeat the analysis with a single-phase fault /59/. The ratio k can then be found from the expression:

$$I_{k1} = I_{k3}\frac{3}{2+k}.$$

This time it is the pole that opens first (pole C) which comes closest to the single-phase situation. This is caused by the fact that the distinctive first reflection against the unloaded transformer on bus 150L is not overshadowed by wave interference as is the case with poles that open later in time.

Fig. 4.12 shows the enlarged TRV for the first pole to clear:

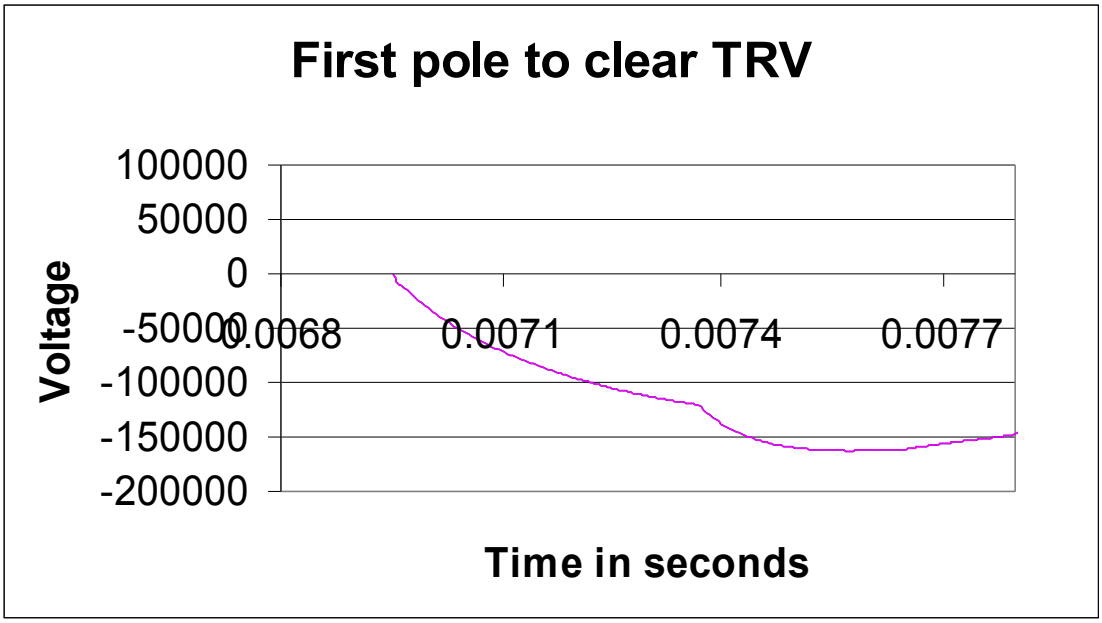

Fig. 4.12 First pole to clear TRV across pole C.

The measured parameters are:

$$S_1 = 100/150 = 0.67 \text{ kV}/\mu\text{s}; \quad \gamma = 162491/178175 = 0.91$$

Compared to the single-phase case (fig. 4.5) we see that the dv/dt is less steep, which finds its cause in the extra (three-phase) capacitances. There is no measurable delay and the TRV has a lower peak factor, caused by extra damping from the other phases and the fact that the phase shift between current and voltage is not exactly 90° - and this is assumed in our definition of γ -.

4.6.6.2.4.Radial Overhead Line Type Networks with an isolated neutral

Although this is not a common situation, i.e. most Overhead Line Type Networks will be effectively earthed, we would like to demonstrate that in such a situation, through the highest First Pole to Clear Factor possible (FPCF = 1.5), this results in extra harsh TRV conditions for circuit-breakers.

The isolated neutral is simulated by a resistance of 1 MΩ on the 300kV level.

Again, as in our ROL Network analyses with solidly earthed transformer neutrals, we will make a short circuit (3LG) on bus 300C with all components connected, including lines. The TRVs are plotted in fig. 4.13.

Since the second and third poles to clear do not open simultaneously, the neutral is not completely isolated and therefore the FPCF is slightly smaller than 1.5. This is caused by the fact that the transformer neutrals at the 525 kV level are solidly earthed and on the 150 kV level they are earthed over a reactance of 12.5 Ω at 50 Hz.

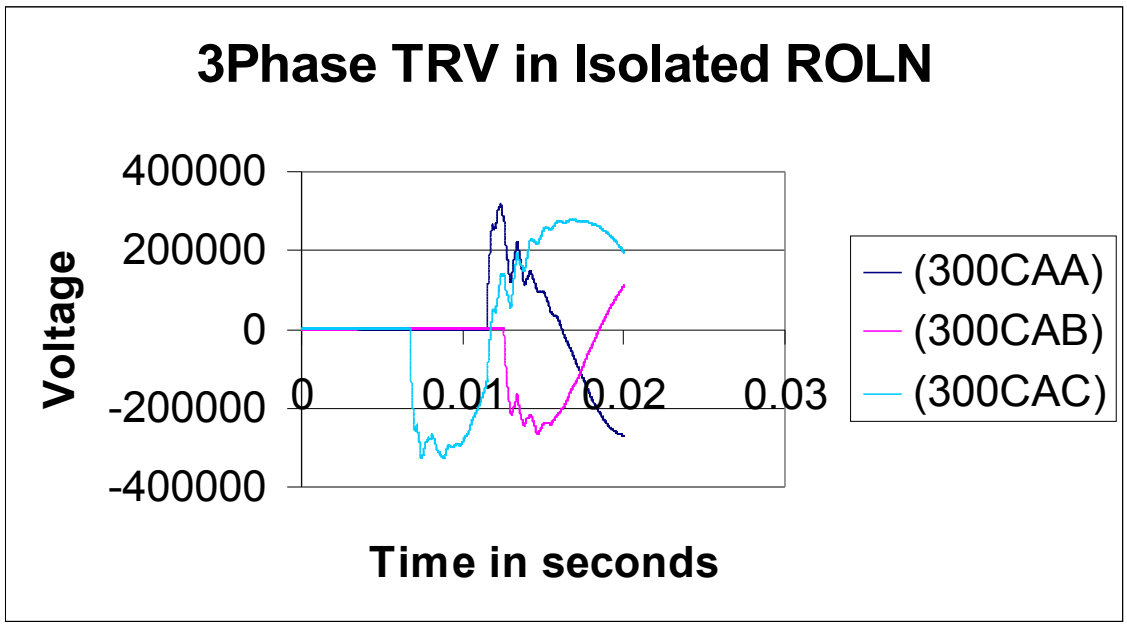

Fig. 4.13 TRVs of a 100% fault (=TD4) in isolated 3-phase 300kV network.

If we compare fig. 4.13 with the TRV's in the situation with solidly earthed neutrals (Fig. 4.8), it will immediately be clear that the first pole to clear (pole C) is stressed more severely, especially dielectrically, since its peak has increased to over 325kV (was about 200kV), as can be seen in the enlarged TRV-plot of fig. 4.14:

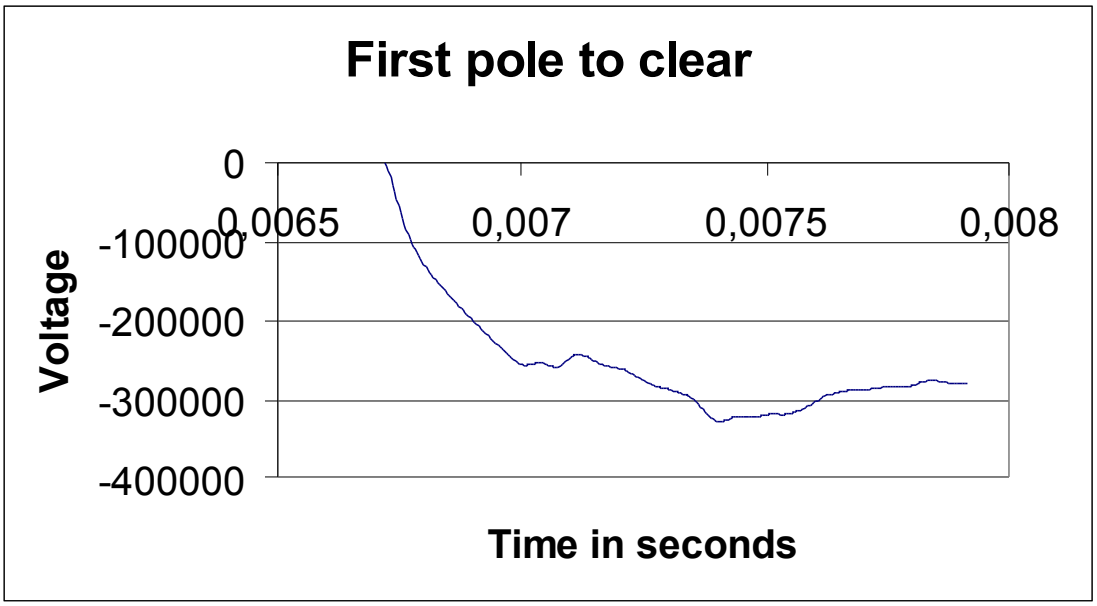

Fig. 4.14 Enlarged TRV of first pole to clear in isolated Network

The measured TRV parameters are:

S_1 = 230/125 = 1.84 kV/µs
σ = 230/390 = 0.59 ; t_1 = 125 µsec
γ = 328/390 = 0.84 ; t_c = 690 µsec
$t_d \approx$ 7 µsec

If we correct these values for the ideal case when FPCF = 1.5 and normalize the values for the IEC definition, we get:

σ_n = 153/245 = 0.62 and γ_n = 219/245 = 0.89

4.6.7Summary on single and three-phase calculations

If we compare the calculated results of the three-phase analyses with the calculated results of the single-phase analyses, i.e. parameters and plots, we see that they do not differ too much, apart from typical three-phase effects like pole to clear factors, extra damping and more dominant wave interference.

We can conclude that we can use the results of the single-phase analyses for a comparison with the standards.

4.7 Consequences for the Three-phase Test Method ?

In literature several system configurations and system faults have been analysed globally and in depth, but the values for the different parameters which quantify a TRV were indicative and often on the low side.

The performed calculations from the benchmark system lead to a clear difference in comparison with the IEC values.

4.7.1Comparison between IEC 4-par values and the calculated results

In table 4.13 TRV parameters from simulations are tabled together with the corresponding IEC values. In the '3PTM' row new proposed values are tabled.

Test Duty 4/5	*S1*	*Td*	*U1*	*T1*	σ	*Uc*	*Tc*	γ
IEC 145kV	2.0	2	-	77	1.3	-	231	1.49
Cable 150kV	6.5	2		23	1.37		192	1.40
3PTM: 100 – 170kV	6.0	2		25	1.3		200	1.50

Test Duty 3	*S1*	*Td*	*U1*	*T1*	σ	*Uc*	*Tc*	γ
IEC 145kV	3.0	2-13	-	51	1.3	-	230	1.59
Cable 150kV	8.5	2.4		25	1.63		84	1.65
3PTM: 100 – 170kV	8.0	3.0		25	1.5		90	1.60

Test Duty 4/5	*S1*	*Td*	*U1*	*T1*	σ	*Uc*	*Tc*	γ
IEC 300kV	2.0	2	-	159	1.3	-	477	1.49
Radial 300kV	6.0	7		47.5	0.86		500	1.49
3PTM: >=245kV	6.0	7		50	1.0		500	1.50

Test Duty 3	*S1*	*Td*	*U1*	*T1*	σ	*Uc*	*tc*	γ
IEC 300kV	3.0	2-22	-	87	1.3	-	392	1.59
Radial 300kV	6.8	7		25	1.42		416	1.59
3PTM: >=245kV	7.0	7		25	1.35		392	1.60

Table 4.13 Comparison between IEC, calculated and proposed TRV parameters.

Note that normalized values σ_n and γ_n are used for σ and γ, since these can be compared best with current IEC values.

4.7.2Proposal for 'adjusted' parameters for Test Duty 3, 4 and 5.

As becomes clear from our 3PTM rows the proposal is to deviate considerably from the current IEC values.

The reason is that we find clear differences between the current IEC values, the values found in literature and the calculated results from the benchmark system.
The escape clause in IEC-60056 (1987, p.51):
"In case of single-phase systems or where circuit-breakers are for use in an installation having more severe conditions, the values shall be subject to agreement between manufacturer and user, particularly for the following cases:……", should of course only be used in exceptional cases,

and not for cases like 'Circuit-Breakers directly connected to Transformers without appreciable additional Capacitance' and the like.

Note: the word 'severe' in the quoted line from IEC is not defined in any particular way.

Of course such an escape clause must be added, but it would be much better to distinguish between:
- thermal severity, with parameters from SLF and/or ITRV duties and
- dielectric severity, to be defined by S_1, σ/t_1 and γ/t_c.

This reasoning is still based on the assumption that there is something as 'a most severe circuit', irrespective of the circuit breaker and its interrupting characteristics, but it is still much better than using the word severe without defining it at all.

A possible way to define 'thermal severity' would be to standardize a SF6 Circuit Breaker Model with fixed parameters and to define a minimum SLF and/or ITRV Epa, to be found by numerical analysis in an available transient analysis tool such as EMTP or X-trans.

This, however, would be a complete deviation from the methods accepted and applied in the past and would therefore be difficult to get accepted.

For Test Duties 4 and 5,

A)
Since the Rated Rise of Recovery Voltages (RRRVs) for Test Duty Nos. 4 and 5 in a Radial Overhead Line Type Network (Voltage ratings: 245/300/362kV) are higher than in the current IEC, TRVs in ROLTNs can be more severe in the thermal regime (higher Epa) than the IEC TRVs.

TRVs in Radial Overhead Line Type Networks are definitely more severe in the dielectric regime and especially 3PCBs must be tested for their dielectric withstand capability.

The thermal behaviour of a 3PCB, however, is reliably tested with SLF tests since this is thermally still more severe than in any comparable BTF situation.
The dielectric behaviour is accurately tested with the higher TRV values present in Radial Overhead Line Type Networks.

B)
For Cable Type Networks (voltage ratings: 100kV up to and including 170kV) it would be best to do a similar thing.

Although both 'weak' TRVs with no delay time and TRVs with high RRRVs and time delay can be more severe in the thermal regime than standard TRV ratings, this is very well tested with a SLF test.

Because the BTF is best suited to test the dielectric behaviour, we will use the higher S_1 and σ values to test the dielectric regime in a BTF test but using IEC TRV-peak values γ.

For the Short Circuit Currents,

C)
As a consequence of the changing Power Density in both Overhead Line Type Networks and Cable Type Networks, a 3PCB has to cope with a higher DC-component in the short circuit current.

Therefore a 3PTM must be able to supply these currents together with rather long AC Recovery Voltages in order to test a 3PCB for its dielectric withstand capability.

A DC-component of at least 50% will therefore be used.

However, if we want to test the 3PCB for its thermal behaviour in the same test, we shall have to take care that the correct di/dt is provided to the breaker at current zero.

For Test Duty No 3,

D)
This Test Duty was originally meant to test a circuit breaker for its dielectric behaviour and we should aim for high TRV peak values.

The TRVs generated at approximately 60% of the rated short circuit current in both Radial Overhead Line Type Networks and Cable Type Networks, have higher RRRV than the current IEC values.
Their normalized peak values (γ_n) are similar to the current IEC values.

Therefore the proposal is to test with the higher S_1 and σ values and retain the standard TRV peak values as currently prescribed in IEC.

For the thermal interrupting capability (SLF Test Duty),

E)
On the basis of our findings in this chapter we can retain the SLF Test Duty as it is defined in IEC.
For SF6 puffer or rotary-arc type breakers commonly in use today the thermal interrupting capability depends strongly on the current to be interrupted.

Especially a lower current produces no or almost no *nozzle clogging*, an effect often used to improve the interrupting capability of SF6 circuit breakers.

A 60% SLF Duty should, therefore, be reintroduced to give this breaker type the opportunity to show its ability to interrupt under these system conditions.

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5 A PROPOSAL FOR A THREE-PHASE LUMPED ELEMENT TEST METHOD (3PTM)

5.1 Introduction

In the previous chapters we concluded that a circuit breaker has several failure modes (Chapter 3, fig. 3.1):

1. A circuit breaker can run into a 'mechanical' failure during the high current interval,
2. A circuit breaker can have a thermal failure during the interaction interval and
3. A circuit breaker can experience a dielectric failure in the Transient Recovery Voltage and the Recovery Voltage interval.

This distinction, especially between thermal and dielectric failure modes, has not always helped in understanding the behaviour of the electric arc /32/.

Although many decades of intense study have brought us more insight towards the inner processes of the switching arc, one is still not able to design a new breaker type without extensive testing in the laboratory.

Testing remains necessary to (re)assure that a circuit breaker is able to cope with different switching conditions. This has been common practice since the early days of electrical power generation and distribution.

A switching arc is a plasma channel in which many specific energy exchange processes struggle for survival. Since it is nearly impossible to describe and model these different processes down to the atomic level for all atoms involved /40/, it is physically unlikely that testing becomes unnecessary in the foreseeable future.

The basic aim of testing is to make sure that a specific circuit breaker will not fail in actual service because of one of the above failure modes.

5.2 Historical Overview

The first 'circuit breakers' were open air switches or used a mixture of oil/water as an extinguishing medium as e.g. J.N. Kelman in 1901 for a 'double barrel' breaker with a rating of 40 kV and 200-300 A.

Testing was done by putting the equipment in actual service and checking whether it functioned or not.

This practice, although simple in its approach, had to be abandoned rapidly since a continuous flow of power to customers and loads during tests could not be guaranteed.

In 1911 it was AEG in Germany that built the very first 150 MVA high power testing station in the world /a,cc/.

And it was around 1920 /x/ (1925 according to Slamecka /b/), that J. Biermanns proposed to use a higher voltage than the power frequency voltage to test circuit breakers by means of his so-called: 'Kunstschaltung'.

In 1929 the Cigre Study Committee on Circuit Breakers started to formulate unified definitions for circuit breaker ratings which at first were meant to cover power frequency components only /c/.

In 1931 Biermanns improved his 'Kunstschaltung' by adding a transformer which, after interruption of the short circuit current, automatically switches a high voltage across the test breaker contacts /b/.

In that same year E. Marx (1931 /b/) proposed to use a charged capacitor to test the test breaker with an impulse voltage.

In 1933 the idea of defining the shape of the recovery voltage was put on the agenda when the Study Committee on Circuit Breakers included the Rate of Rise of the Recovery Voltage in their annual report /c/.

As early as in 1935, as a result of field tests, it was accepted that the Recovery Voltage could not be defined by one parameter only, for instance by the rate-of-rise /c/.

It was Skeats who, in 1936, proposed to use a spark gap to improve the Biermanns circuit of 1931 /d/.

In 1942 Weil came with the idea to apply the Marx principle and to let the charged capacitor generate a 'high' frequency oscillating current which was switched on to the Test Breaker (TB) at precisely the right moment by the use of a spark gap, so that the TB would interrupt this current as if it were a normal short circuit current.
The resulting TRV would swing towards the charged voltage of the capacitor, which could then reach a higher value than the driving voltage of the high current circuit.

With the introduction of this test circuit, the so-called: 'equivalent' synthetic testing of high voltage circuit breakers became possible, especially when in the 1950s circuit breaker power rapidly began to surpass direct testing power /z/.

The Weil circuit was further improved upon by Dobke, Bloemecke and Slamecka, resulting in the well-known Weil-Dobke or parallel current injection synthetic test circuit.

Other test schemes, which also attempted to tackle the problem of an *Unpaused Stressing* of the TB in the overlap from the high current phase to the high voltage phase (TRV), such as the voltage injection scheme, were developed as well, as can be learned in the excellent book by Slamecka on this subject /b/.

The problem of 'Unpaused Stresses' and 'Equivalent to Direct Tests' remained high on the agenda for a long time /u,v/, but was never solved to complete satisfaction.
Study committee members agreed, however, that the Weil-Dobke circuit was the 'most equivalent' of all test schemes.

Several of these test circuits were used in High Power Laboratories (HPLs) around the world. Nearly all of them were built and/or improved in the time period between the 1930s to the 1960s, as is recorded in /b/ or in references referred to in /b/.

With the (re)introduction of Three-Phases-in-One-Tank Type Circuit Breakers (3PCBs) in the mid 1970s, the testing practices in use at that

time were insufficient since additional failure modes - like inter-phase and phase to tank interactions – were not covered.
Three-Phases-in-One-Tank Type Circuit Breakers had been in use before. E.g. in the very beginning of circuit breaker development, in 1901, BBC had a hand operated oil circuit breaker with all three interruption contacts, without any form of seperation, in one tank /cc/.

The first SF6 insulated 3PCBs on the Market had a breaking capacity of 145kV/31,5kA in 1975 or 84kV/31.5kA in 1976. So the three-phase direct testing method, which should preferably be used, was already beyond the capabilities of almost all test stations.

Due to the rapid increase of the breaking capability to 300kV/50kA in 1986 and higher it simply became impossible to use this direct testing method in any High Power Laboratory at all.

To tackle this shortcoming in testing techniques, several new synthetic test circuits and/or test procedures were introduced in literature.

An overview of the advantages and disadvantages of these test schemes in chronological order:

Case A. Bitsch, Richter and Schramm, 1976

One of the first test schemes was proposed by Bitsch, Richter and Schramm from Siemens in 1976 /e/ (for a circuit layout refer to the Appendix II Figure A).

This scheme was a further improvement on /aa/ where the TRV was injected in one phase at the time only.

The scheme is based on two-part testing.
- Part I is a three-phase recovery voltage test which, essentially, is a direct Skeats derivative to test the long term dielectric withstand capability and
- Part II is a single-phase voltage injection test to verify (for one phase only) the thermal and dielectric (TRV) recovery and withstand capabilities.

An advantage of this circuit is that the late dielectric phase, which is important for a 3PCB, is correctly stressed by an AC Recovery Voltage.

A disadvantage is that the thermal phase and TRV dielectric phase are tested single-phase only and even then with a voltage injection scheme, which, because of circuit breaker stochastic behaviour, can be thermally more severe than in a direct test.

Case B. Damstra and Kempen, 1980

A similar circuit was proposed by Damstra and Kempen in 1980 in /f/ (for circuit layout see Appendix II Figure B), which they named the ‘Three-phase transformer injection circuit’.

Where Bitsch et al. in fact make use of a three-phase Skeats circuit with one power source for both the high current and the high voltage circuit and omit triggering devices, Damstra and Kempen make use of switches (specially developed triggerable vacuum injection gaps) to control the high voltage circuit and use two power sources: one for the high current circuit and one for the high voltage circuit.

This scheme has the advantage that the buildup of voltage after current interruption can be controlled. First the high current supply circuit generates the first part of the TRV right after interruption then at the right moment the high voltage circuit is switched automatically onto the test breaker by a voltage level detection circuit to generate the full TRV.

The circuit has the same advantages as the Bitsch scheme, but the disadvantage is that it is in fact a three-phase voltage injection scheme which, as we learned from our analysis in Chapter 2, could be more severe for the breaker in the thermal region than a direct test. It also requires three injection gaps and automated control circuits.

Case C.Azumi et al., 1979

In 1979 Azumi et al. published another method /g/ (for the circuit layout see Appendix II Figure C).

In this scheme the same short circuit current flows through all three phases but the TRV is applied to only 'two' phases by a parallel current injection circuit (Weil-Dobke).

The advantage is that three phases carry the full short circuit current and that for 'two' phases the thermal mode is correctly tested.

The disadvantage is of course that only the two first clearing phases are subjected to the TRV and the subsequent recovery voltage simultaneously and this recovery voltage is not a full power frequency recovery voltage but a damped AC oscillation.

The latter problem is overcome by a scheme proposed by Ibuki et al. /bb/ or /r/ in 1988. By means of a transformer extension a real AC recovery voltage is put onto pole 'W' (see appendix).

Case D.Manganaro, 1980

In the 1980 Cigre Group 13 Session discussion on three-phase synthetic testing Manganaro elaborates on the circuit in use at CESI (Italy) /h/ (see for circuit layout Appendix II Figure D).

This scheme makes use of the Weil-Dobke parallel current injection circuit to test for the first pole to clear the thermal and dielectric modes. The last two poles to clear are stressed by nominal AC Recovery Voltages.

The advantage is that the first pole to clear is stressed correctly in the thermal and TRV dielectric mode and also an artificially created AC recovery voltage is applied. Another advantage is that the two last poles to clear are stressed by a transformer TRV and an AC recovery voltages for a sufficiently long time.

The disadvantage is, of course, that the thermal mode is only tested single phase and that the TRV dielectric mode is only tested in this phase with a 4-parameter TRV and not for the other phases. Besides that, the recovery voltage on the first pole does not have the correct AC wave shape.

Case E. Berneryd, 1981

At a special meeting of the CEA Engineering and Operating Divisions, held in Toronto in 1981, Berneryd reviewed several methods /i/.

* He discusses the until then often applied single-phase methods, being the:
- Weil circuit;
- Voltage injection; and
- Skeats circuit

Of course all methods are adepted for three-phase testing with a full three-phase high current supply and one of the high voltage injection methods in one phase only.
Berneryd comes to the conclusion that the combination method of a full three-phase current and a parallel current injection scheme (Weil circuit) in one phase is the best to use.

In order to be able to test for most of the failure modes Berneryd proposes a multi-part test procedure with minor and major loops of an asymmetrical AC current.

To overcome the "classical" drawback, voltage in one phase only, he proposes to inject in each phase by turn.

Because the thermal and dielectric behaviour is more or less correctly tested in the pole to which the high voltage circuit is connected, the advantage is that the scheme is relatively simple and can be used in several testing stations.

The disadvantage is of course that only one pole at the time is stressed by both voltage and current.

At the Toronto meeting Berneryd also discusses circuit patented by Slamecka in 1977 /j/.

The Slamecka circuit uses the Voltage Injection Scheme by stressing the first pole to clear with a Voltage Injection Circuit and the second and third poles to clear by a second Voltage Injection Circuit.

Apart from the fact that the need for two injection circuits restricts its application to a limited number of High Power Laboratories, it can only be used for a First Pole to Clear Factor of 1.5.
Berneryd criticizes that the thermal failure mode is probably not correctly tested by the circuit.
This observation is supported by an Epa analysis on the Voltage Injection Test Circuits. The conclusion can be drawn that the Voltage Injection Test Method most probably overstresses the breaker under test in the thermal region.

Berneryd also pays attention to the Bitsch Scheme /e/, the Damstra&Kempen Scheme /f/, the CESI Scheme /h/ and the Azumi Scheme /g/.

Case F. Nakanishi, 1982

In 1982 Nakanishi and others /k/ propose a test circuit (for the circuit layout see Appendix II Figure F) which resembles the circuit of Azumi /g/.

Instead of using one phase of the test breaker as auxiliary breaker (AB), an additional single phase AB is doing the job.
In this scheme only one phase is subjected to a Breaker Terminal Fault (BTF) related TRV, generated by a Weil-Dobke circuit, and the three phases are stressed by a three-phase current supply.

This circuit has the advantage over the circuit of Azumi that it does not overstress the breaker (during the dielectric recovery period) since only one pole is stressed as first clearing pole.

The Nakanishi circuit has the same drawback as the Azumi circuit because not all three phases are stressed by a TRV and a RV and because the RV is not really an AC-Recovery Voltage.

Nakanishi et al. also compare the Azumi circuit /g/ and other circuit proposals for testing the dielectric withstand capability between phases and tank after current interruption.

One circuit employs a Marx generator to one of the phases after the other two phases have been subjected to the short circuit current to test this phase for its peak voltage withstand capability.
Another circuit makes use of a single phase transformer injection circuit after the other two phases have cleared the short circuit current to test this phase for its AC recovery voltage withstand capability.

Case G.Yamamoto, 1984

In 1984 Yamamoto and others describe a test circuit which supplies the correct short circuit current to three phases and a correct TRV and RV to the second and third poles to clear in an ungrounded system having a FPCF = 1.5 /l/ (for a circuit layout see Appendix II Figure G).

Yamamoto states that in an ungrounded three-phase system the TRVs for the second and third poles have a higher peak value than the first pole to clear. Also the arcing time is longer and therefore the second and third poles to clear face more current stress and a higher dielectric stress than the first pole to clear.

A charged capacitor is used to generate a high frequency current oscillation, which stresses the second and third poles to clear with the right TRV and AC RV through a transformer.

The circuit has the advantage that after the three-phase current stresses, correct TRVs and RVs are applied to the second and third poles to clear.

The drawback is that the first pole to clear is tested neither thermally nor dielectrically and that the scheme can be used only for ungrounded system faults because the second and third poles interrupt at the same time.

Case H.Van der Linden and van der Sluis (KEMA), 1986

In 1986 van der Linden and van der Sluis (KEMA) publish a circuit tuned to the capabilities of the KEMA Lab /m/ (for a circuit layout see Appendix II Fig. H).

They use two Current Injection circuits to stress both the first and second/third pole to clear with the right thermal and dielectric TRV stress. The recovery voltage is generated by the Current Injection circuits themselves and this causes a decrease in amplitude in a rather short period of time.

The advantages of the KEMA circuit are that the first pole to clear is correctly stressed for the thermal failure mode of the breaker and the TRV-dielectric failure mode and that the second and third poles are stressed correctly both thermally and dielectrically during the TRV period.

But a FPCF lower than 1.5, as is the case for grounded faults in grounded systems, cannot be covered by this circuit.

The recovery voltage is not a full AC recovery voltage and similar to the Froehlich scheme (see hereafter) the circuit is rather sophisticated and requires a well-equipped test station with appropriate control and timing circuits.

Case I. Froehlich, 1987

In 1987 Froehlich et al. /n/ published a rather sophisticated circuit (for circuit layout see Appendix II Figure I).

Apart from correct thermal stresses for the second and third poles to clear this circuit covers every aspect of three-phase circuit breaker testing.

It makes use of a single Current Injection circuit for the thermal and TRV-dielectric stress on the first pole to clear and two Voltage Injection circuits to apply the TRV-dielectric stress on the second and third poles to clear. The RV is supplied by a three-phase Skeats scheme.

In order to test at longer arcing times Reignition circuits are used in all three phases.

Apart from the fact that the second and third poles are not stressed with the correct thermal stress, it should be noted that the operation of the circuit is rather complicated and that three injection circuits are necessary and therefore it can not be used in the majority of the High Power Laboratories.

Case J. Cigre WG 13.04 and IEC SC 17A, 1989

In 1987 Cigre Working Group 13.04 /o/ and in 1989 IEC Study Committee 17A Working Group 10 /p/ published contributions on the topic of synthetic test methods for 3PCBs.

The Cigre paper contains five (5) requirements which should be fulfilled in order to be able to speak of a correct 3PCB Test Procedure. In short these requirements are:

- Full three-phase current should be supplied to the 3PCB under test.
- Arc duration in all three phases must correspond to the ones occurring under three-phase direct test conditions. It is permitted to make use of arc reignition circuits (ARCs) in order to be able to meet this requirement.
- A synthetic circuit capable of producing correct current and voltage stresses must be applied for the first pole to clear.
- The TRV between the last clearing poles and the metal enclosure must have a proper amplitude and phase relation. This can be achieved by using synthetic test circuits for which the parameters of equivalence during the interaction interval do not necessarily meet all the requirements.
- The recovery voltage should be applied during a proper period of time and across at least two adjacent phases.

Furthermore Cigre and IEC contributions analyse many of the - by then - known three-phase test circuits with respect to their five requirements: Injection in one phase /Nakanishi/, Injection in all phases /Froehlich, van der Sluis and van der Linden/, two-phase circuit /Azumi/, three-phase Skeats circuit /Bitsch/ and the combined circuit /Manganaro/.

In Appendix HH to IEC-60427 /p/ published by IEC SC 17A WG10 eight (8) requirements are described:

- Full three-phase current shall be supplied to the 3PCB under test.
- Sub-clause 6.102.9 of IEC-60056 shall be fulfilled. This is a long clause on proper arcing times for 3PCBs.
- To verify thermal behaviour between the terminals of the pole(s) proper synthetic circuits shall be used, such as the parallel current injection method.
- The TRV between at least two clearing poles shall have the proper amplitude and phase relation. This can be obtained by using synthetic circuits for which the interaction interval may be relaxed.
- The recovery voltage shall preferably be a.c. and shall be applied during a proper period of time and across at least two clearing poles. The RV shall have the proper amplitude and phase relation.
- In order to be able to test within the maximum permissible period of time between tests – IEC-60056 sub-clause 6.105.1 - of a test series, it is allowed to reproduce all the required arcing times on the same phase.
- The enclosure shall be grounded at one point only.
- All the above stresses should preferably be applied in the same test, but multi-part testing is allowed.

Some of the requirements are a relaxation of real three-phase stresses, such as the requirement that: 'The Transient Recovery Voltage between at least two clearing poles shall have the proper amplitude and be in correct phase relation ……. This can be obtained by the use of synthetic circuits for which the requirements *during the interaction interval may be relaxed*.'

But other requirements result in an *increase* in stresses applied to the 3PCB, such as the requirement that: 'The Enclosure shall be grounded at one point only.'

In Appendix HH many test circuits are discussed as well:
the Three-phase transformer injection circuit, the Combined circuit, Injection in one phase, Injection in all phases, the Two-phase circuit and the Three-phase duplicate or Skeats circuit.

Case K. Yamashita et al., 1989

In 1989 Yamashita et al. analyse the transient and power frequency voltage stresses for a 3PCB operating in an Effectively Grounded System (EGS) or a Non-Effectively Grounded System (NEGS) /q/.

Yamashita comes to the conclusion that especially the dielectric stress from the recovery voltage between the second and third poles and between these poles and the tank are most severe.

The proposed test method (for circuit layout see Appendix II Figure K) is a two-part test in which the first pole to clear is tested in a conventional way. The second and third poles to clear, both for NEGS and EGS, are tested in a separate test circuit by means of a standard three-phase current phase followed by a transformer voltage injection scheme using a current injection circuit for the correct TRV and RV on the second and third phase and the tank.

The test method makes use of the transformer voltage injection circuit with a charged capacitor to apply the TRV because the authors emphasize that a high extinguishing peak is of influence on the peak of the TRV in a Skeats set-up.

The advantage of their approach is that the second and third poles to clear are stressed by 'correct' Transient Recovery and Recovery Voltages but the disadvantages are that the first clearing pole is tested without correct inter-phase and phase-to-tank voltages and in the second part of the test the first clearing pole is not stressed by a realistic TRV and RV.

Also in 1989 Nakamoto et al. /y/ discussed the same circuit at a Cigre colloquium in Sarajevo.

They made an interesting remark about three-phase testing:

- "By analyzing a hot-gas flow it was found that a 100% BTF test is the most severe condition for the insulation between phases and the tank."

Case L. Nakanishi, 1990

In 1990 Nakanishi et al. reviewed several circuits which were by then in use by different Japanese companies /r/.

The Yamashita /q/ circuit is analysed and the Azumi circuit /g/ is also discussed.

Nakanishi focuses on the intense interaction of the physical processes in a 3PCB and compares the circuits to the Cigre requirements as laid down in /o/.

All circuits make use of one or more of the 'escape' clauses in the Cigre document /o/ in order to fulfil the requirements, without doing a full three-phase test.

Case M.Yoshizumi and Sugiyama, 1990

During a CRIEPI-STL Meeting in 1990 Yoshizumi and Sugiyama discuss specific three-phase interruption characteristics for both current and voltage in effectively earthed (FPCF=1.3) and non-effectively earthed (FPCF=1.5) systems and also focus on the intense interaction between the physical processes inside the 3PCB /s/.

Except that the paper describes the test methods already used in practice, it also analyses the methods in relation to their findings for three-phase characteristics and intensified interactions inside a 3PCB.

They analyse: Nakanishi 1982 /k/, van der Sluis and van der Linden 1986 /m/, Bitsch 1976 /e/ which they think was written by Ruoss 1987 /o/, Damstra and Kempen 1980 /f/, Yamashita /q/, combined circuits discussed by Ruoss /o/, Froehlich 1987 /n/ and Ibuki 1988 also discussed in /r/.

Furthermore they discuss some Japanese circuits like Kawasaki 1979, Morita 1985 and Kuzuma 1987, all of which are variations on a general theme: they use some kind of relaxation clause in order to be able to test in equivalence with a direct three-phase test.

The published analysis of the 'Skeats' circuit (Bitsch) needs an amendment because the authors state that the scheme does not need synchronization, but this was found not to be true as will be explained later.

Case N.Van der Sluis et al., 1990

In a paper presented at the 8th CEPSI Conference in Singapore 1990 vd Sluis et al. /t/ present test results on a 145kV/40kA 3PCB operating in a

isolated system (FPCF = 1.5) and which was tested with the circuit discussed in /n/.

This paper shows that the test circuit can be successfully used to test practical 3PCBs, in spite of the necessary complex control circuits and the three-phase auxiliary breaker.

Case O.IEC SC17 Sub 17A : IEC 61633, 1995

In a so-called type 2 publication, which is open to criticism but is expected to meet consensus in a not-too-distant future, IEC SC17 sub-committee 17A prepared the proposal IEC 61633: 'HIGH-VOLTAGE ALTERNATING CURRENT CIRCUIT-BREAKERS-GUIDE FOR SHORT-CIRCUIT AND SWITCHING TEST PROCEDURES FOR METAL-ENCLOSED AND DEAD TANK CIRCUIT-BREAKERS' /w/ in 1995.

The publication first analyses the special nature of a multi unit and/or multi phase in a one-enclosure type circuit breaker.
It mentions the intense mechanical, electrostatic, electro-magnetic and gas-dynamical interaction between the interrupter units of a single pole or the interrupters of the different poles.

Since this breaker type is expected to change rapidly in a way that is hard to predict, a very general escape clause is given:
"If a special interaction is eliminated in a given design, it is no longer necessary to adjust the tests to cover this interaction. In that case, it is necessary to demonstrate that the interaction under consideration has negligible influence on the test results, which could be made by model calculation, or experimental demonstration, using special measuring techniques."

According to this clause any agreement between the client and manufacturer meets this 'standard' since in fact nothing is defined.

In a special Chapter on 3PCB testing is stated that if direct testing is possible, the direct tests covers all possible stresses.

This implies that present stress ratings as specified per standing IEC are automatically correct and that worsening of network conditions, as we have found in the chapter on stresses, is not taken into consideration.

When synthetic testing is applied, five requirements must be fulfilled.

The requirements are rather simple in their description but some clear boundaries are defined:
- full three-phase current must be applied,
- TRV and RV stresses are given and neatly organized in tables and
- preferably all stresses should be covered in one test. If this is not possible, multi-part testing is an allowed procedure.

The last clause opens the door for a different testing approach.

Test Duties 1,2 and 3 are allowed to be performed single-phase, but for TD5 the recovery voltage must be AC.

The clause also mentions that the SLF test can be performed single-phase. This circumvents the aspect that a 3PCB, especially equipment with a common drive mechanism, is influenced by three-phase current, three-phase capacitances and possibly by three-phase magnetic crossover influences.

As examples of synthetic test circuits that can be used, only some primitive circuit layouts are discussed:

- Three-phase transformer injection circuit (like Damstra and Kempen)
- Combined circuit (like CESI)
- Injection in all phases (like KEMA or Froehlich without AC RV)
- Three-phase duplicate circuit (like Bitsch)

For the duplicate circuit the comment is given in a note that it can only be used for dielectric tests and therefore can only be applied in the case of multi-part testing.

As will be shown later, the duplicate circuit can be used for dielectric tests quite conveniently, but - of course - still has certain deficiencies.

5.3 Requirements for a Three-phase Test Method.

The Introduction and the section with the Historical Overview make it clear that testing has matured in line with circuit breaker development, be it with an understandable time lag.

It took for instance a 15-year period before the two and four parameter method for defining TRVs was incorporated in IEC-60056, after its first publication by Hochrainer in 1957 /1/.

In the United States of America the two and four-parameter TRV wave formulas were never accepted, even though it was acknowledged in a publication from the IEEE that the method was better than their own /2/.

Testing practices are always "under construction" and proposals for changes do arise quite often, but usually they constitute a minor change.

Ragaller and Reichert, however, propose a more or less complete departure from standard testing practices in /5/. By means of limiting curves, they make clear that a breaker can have either one of the two failure modes: a thermal or dielectric. When operating under certain system conditions one of the modes limits its operation, but the other failure mode will not occur and therefore they state that;
'…… with the aim of avoiding uneconomical test expenditures. For example, it makes little sense to prescribe a large number of short-line fault, and perhaps even itrv, tests for a breaker that is supposed to operate above the intersection point of the two limiting curves. Such a breaker will never be limited by the thermal interruption mode, unless it is used at a lower network voltage'.

Ragaller and Reichert propose to use this approach for testing *every* Circuit Breaker put into service only for its limiting failure mode under the actual Network conditions in a routine test.

Comparable we propose to use a similar approach to use the least amount of *type tests* to prove the ability of the circuit breaker to withstand 90% of practical system conditions.

"We know it is quite a risk to propose a complete overhaul of testing practices but we are young and bold enough to hope to see the days that …", A.J.P. de Lange, 2000.

We propose to test for the different failure modes in different tests, i.e. a kind of two-part test procedure:

1. A test for the thermal failure mode with a three-phase SLF-test and
2. A test for the mechanical failure mode and dielectric failure mode(s) with another test circuit.

Such an approach was already proposed for 3PCBs, by Tominaga (Japan) in the Cigre Working Group 13 Session of 1980 /6/ and also by Berneryd in 1981 /7/ and both Cigre and IEC accept such a scheme under certain conditions /8,9,10/.

Such a test practice is allowed for 3PCBs (filled with SF6) since the thermal failure mode can be treated on its own because it does not influence the other failure modes.

Support for this is given in the book on SF6 breakers by Ryan and Jones /11/. They state that: " The thermal-recovery period of SF6 interrupters persists for a short time of the order of 4μs either side of the current zero and at the end of the current wave. Because of the short time duration involved, it is predominantly the condition and behaviour of the contracted arc column (Diameter ~1 mm), rather than processes remote from the arc, which dominantly govern the thermal recovery."

Since the high current phase (mechanical failures) is followed by the thermal phase, which in its turn is followed by the dielectric recovery period, influencing can only be in that order.

Therefore the following the question can be raised:

- "Does the high current phase influence the thermal and/or the dielectric phase ?"

The answer is, it influences both.

The high current phase has its influence on the thermal phase by means of the di/dt at the instant of current interruption /5/.
It also determines the available active cooling power at the moment of interruption. This can be quantified by the minimum and maximum arc time the so-called: *extinguishing window*.

The high current phase also has a significant influence on the dielectric withstand phase because of the amount of hot gas and debris being produced /5/ and it influences the dielectric recovery phase by the di/dt as can be read in /12/.

On the question:

- "Does the thermal phase influence the dielectric recovery period and/or dielectric withstand period ?"

The answer should be: no.

A support for this answer is that circuit breaker testing was done by means of rather simple single or double frequency TRVs between the 1920s to 1960s, but these TRVs do *not automatically* stress the breaker in the thermal region as we do know now after the Epa analysis in chapter 4.

In the 1950s several circuit breaker failures were definitely not caused by mechanical or dielectric failures and there were doubts about the 100% coverage of the single or double frequency TRVs to cope for all circuit breaker stresses.

Then for a period of 20 years the Short Line Fault (SLF) was put on the agenda, at first as a network phenomenon and later for analyzing what effect it has on the switching arc.

For a dielectric failure two mechanisms act together: hot gasses in combination with a relatively large voltage difference over a not too long distance.

This makes it clear that the high current phase can influence the dielectric phase, since during the high current phase a large amount of thermal and chemical energy is 'stored' in the gas plasma by heating and decomposition.

The amount of energy stored in the gas plasma at current zero is typical in the order of:

$$U_a * I_{eff} * \tau_{cassie} = 1\ kV * 50\ kA * 100\ \mu sec = 5\ kJ \qquad \text{(Eq. 5.1)}$$

and the amount of energy stored in the plasma channel during the thermal phase, after current zero, is in the order of:

$$TRV * I_{pa} * \tau_{mayr} = 5\ kV * 100\ mA * 1\ \mu sec = 0.5\ mJ \qquad \text{(Eq. 5.2)}$$

A difference of 7 orders of magnitude ! And this makes it clear that the thermal interval is of negligible influence on the dielectric recovery period and/or dielectric withstand period.

Even the influence of the thermal phase, caused by means of the arc extinguishing voltage peak and the post-arc current on the (I)TRV /5,13,14,15/, is hardly of consequence in the dielectric phase(s), as can be seen as well from equation 5.2 in relation to equation 5.1.

For the test procedure for 3PCBs this indicates that a kind of 'two part test procedure' is quite feasible.

5.4 The 'two-part' test procedure (2PTP).

In the 'the two part test procedure' the high current phase and dielectric recovery and dielectric withstand phase will be tested in dielectric tests in which the circuit breaker shall not fail during the interaction interval.

The high current phase, now combined with the thermal phase, will be tested in another part of the test procedure – the thermal test – in which the 3PCB is not be dielectrically stressed to the full extent.

5.4.1Dielectric tests

As already discussed in the previous section, the dielectric recovery period and dielectric withstand interval are both critically influenced by the high current phase, as can be read in /3,5,12/.

In the chapter on CB-models it has been analyzed that especially 3PCBs are vulnerable where dielectric failures are concerned.

In the Chapter on Stresses it became obvious that particularly 3PCBs in dense High Power Networks may be submitted to very high current stresses: asymmetrical short circuit currents with long time constants.

Therefore the dielectric tests should include at least one test with full

short circuit current having a DC-content of 50% in a supply circuit with a time constant of 100 msec. The extinguishing window must be close to the limits of the test breaker.

Real network current stress will always be in between 50% and 0% DC-content.

It can be read in the paper from Perkins and Frost /12/ that the first stages of dielectric recovery are, like the thermal behaviour, critically influenced by the di/dt.

The RRRV that can be withstood during the first stages of dielectric recovery decreases to about fifty percent when the di/dt doubles.

Tuma /16/ writes that: "The magnitude of the interrupted arc current is expected to influence the dielectric strength of the extinguished arc channel through three mechanisms."

1. The arc mantle created in the high current regime cools down slowly and thereby blocks radiation from the earlier arc channel.
2. Arc channel radius and temperature at current zero increase with the arc current magnitude.
3. If nozzle clogging occurs in the high current regime, and most circuit breaker designs rely on this effect, it increases the flow of cooling gas in the near current regime. The ablation products from the nozzle surface contaminate the arc channel plasma and affect its recovery characteristics.

Perkins and Frost /12/ come to a dependency between maximum current value I_{rms} and the first part of the Transient Recovery Voltage after similar considerations. The frequency and the peak value of the voltage oscillation, in particular the first peak value, correlate with a maximum frequency of the first part of the TRV ('1-cos' wave from) for a particular duty at maximum current.

This reasoning can also be applied to Air-Blast Circuit Breakers as discussed by Hochrainer /17/.

These correlations require a second test in the dielectric part test-procedure, this time with full symmetric short circuit current (DC-content as low as possible, preferably ~0%), since symmetric currents result in the maximum di/dt combined with a steep and high first excursion of the TRV.

So, dielectric behaviour is in fact tested in two testcircuits: one with a maximum asymmetrical current corresponding with IEC Test Duty 5 and one with a full symmetrical current with a steep dv/dt and high first TRV peak duty corresponding with IEC Test Duty 4.

As far as the TRV(s) is concerned, they must include both, the steepest RRRV (S_1) and high first peak value, i.e. high σ, and the highest crest value (U_c) when the grid interacts with a breaker in actual service.

It is an absolute necessity since the dielectric recovery of an extinguished arc column is a complicated process which is influenced by many independent parameters, even to the extent that the voltage *history* up to a certain moment in time plays an important role /11,18/.

In the beginning dielectric recovery is rather quick, within 100 μsec /18,19/ to about 1 per unit (with "unit" being the normal TRV rating), then a slower region is passed which takes from one hundred to several hundred microseconds and the final recovery is again rather fast /18/.

Since the actual withstand capability curve depends on many independent parameters such as di/dt, nozzle geometry, turbulence and RRRV, it is not possible to define a TRV which should test for all specific weaknesses.

Other research into dielectric recovery of the 'afterglow' gives a comparable picture /20,21/.

Instead of testing for all possible weaknesses, defining one or two TRVs that cover maximum network TRV stresses is the more logical route to follow.

As we know from our investigations into TRVs (chapter 4) it is the delay time that influences the thermal severity of a TRV most and overdamped TRVs (4-parameter) usually produce a higher thermal severity than Transformer TRVs (TRF TRVs) because the latter usually have long delay times. However, TRF TRVs produce the highest RRRVs.

Since high RRRVs are critical for dielectric recovery, the test circuit TRV(s) must have both high RRRVs and (high) standard IEC peak voltage ratings to cover maximum Voltage stresses.

This is achieved by using transformer type TRVs (TRF TRVs) because they have a characteristic '1-cos' wave form and a high natural frequency.

The fact that a gradual TRV buildup (*voltage history*), as is the case with 4 parameter TRVs which occur frequently nowadays, causes a better withstand capability during the first fast recovery region, supports this assumption.

To quote the words of Schade and Ragaller /18/: "This means that for the breakdown level after 100 μs it makes a difference as to whether in the earlier phases a voltage was applied or not."

Or as Tuma says /16/: "……, space charge in a hot gas is found to modify the breakdown behavior of the gas, causing it to depart from Paschen curve predictions." And: "The dielectric strength of the arc channel at times larger than 100μs is found to depend on whether a recovery voltage is applied right after current zero or not. … … As a consequence, the free recovery method (Method of doing tests with dc currents. Thereby the TRV is only applied after some delay time, AdL.) is expected to yield a lower value for the dielectric strength of the channel than would be obtained by the ac method (The TRV is automatically applied without a real delay; A. de Lange)."

The effect that a gradual buildup causes a better withstand capability can also be deduced from the fact that, with 4 parameter TRVs, a dielectric failure usually occurs in the region near the peak /5/.

So Transformer/Reactor TRVs are more severe for a SF6 circuit breaker during the dielectric recovery period than overdamped 4-parameter TRVs.

This also shows us that 4-parameter TRVs, as they are standardized now, are less adequate for two reasons:

1. If a Test Breaker does not fail a BTF test (TD4) in the thermal region, with its delay time (t_d) and ITRV requirements, it is still not clear whether it will survive a SLF test duty (for further explanation read Chapter 4) and
2. If a Test Breaker does not fail a standard BTF test (TD4) with a 4-parameter (overdamped) TRV in the dielectric region, with its RRRV and first peak (σ) and final peak (γ) values, it is still not clear whether

it will survive a Transformer TRV at a 100% or 60% current duty, even with identical RRRV, σ and γ, not to question whether it will survive the higher TRF TRV ratings.

To prevent the breaker from failing in the thermal interval during the dielectric tests, the test TRV must have a delay time (t_d) of an order of magnitude longer than the time constant of an SF6 arc. We will therefore choose something in the order of 5 to 10 μsec.

Interpreted in a different way: the delay time must be long enough for the thermal stress (Epa) to be minimized to a value below that of our SLF test (see below).

The recovery voltage (RV) is required to stand for several tens of milliseconds and should be AC (Chapter 4). Therefore we choose it to be present for at least a 100 – 200 msec /34/.

The three-phase Skeats circuit /d/ covers all the above-mentioned dielectric requirements.

To use Skeats for the dielectric regime only is not new and has already been proposed before /7,22/.

The Skeats circuit has many advantages in that it more or less "automatically" produces a 'weak' thermal stress and can produce high values of S_1 and, with some modifications, high values of σ.

Another welcome circumstance is that in a three-phase test set-up the TRVs and RVs for every consecutive pole to clear are automatically correct regarding amplitude and phase relation.

To account for the differences between grounded and ungrounded faults in solidly, effectively, non-effectively or even ungrounded networks, which result in different pole to clear factors for the 1st, 2nd and 3rd poles to clear and in different current stresses, we must have a dielectric part test which generates these pole to clear factors as laid down in IEC for each voltage level.

For the ungrounded faults the first pole to clear factor FPCF is 1.5, for grounded faults in effectively grounded Networks the FPCF is fixed at 1.3. In a modified Skeats scheme this is accomplished by inserting a neutral impedance in the high voltage source, because the test breaker has to be solidly grounded.

To account for an asymmetrical geometry or other asymmetrical effects in the 3PCB, each pole should at one time act as 1st, 2nd and 3rd pole to clear. This can be achieved with reignition equipment.

5.4.1.1.The basic operating principle for the dielectric test circuits

The way in which the dielectric test circuits are configured and are operating in the test sequence is also important.

The circuits must be able to produce steep TRVs that do not stress the breaker in the thermal interrupting interval but must result in a correct amplitude and phase relation.

The supply circuit must be able to supply the 3PCB with three-phase symmetrical and asymmetrical currents.

Another practical requirement for the test circuits is that they operate as simple as possible.

Since the voltage gradient between the contacts influences the dielectric withstand capability, that in its turn is influenced by the potential difference between poles and tank /23/, the tank of the test breaker must be solidly earthed, because this is also the case in practice.

These requirements can in principle be fulfilled with a three-phase Skeats scheme.

The general circuit layout is shown in Figure 5.1.

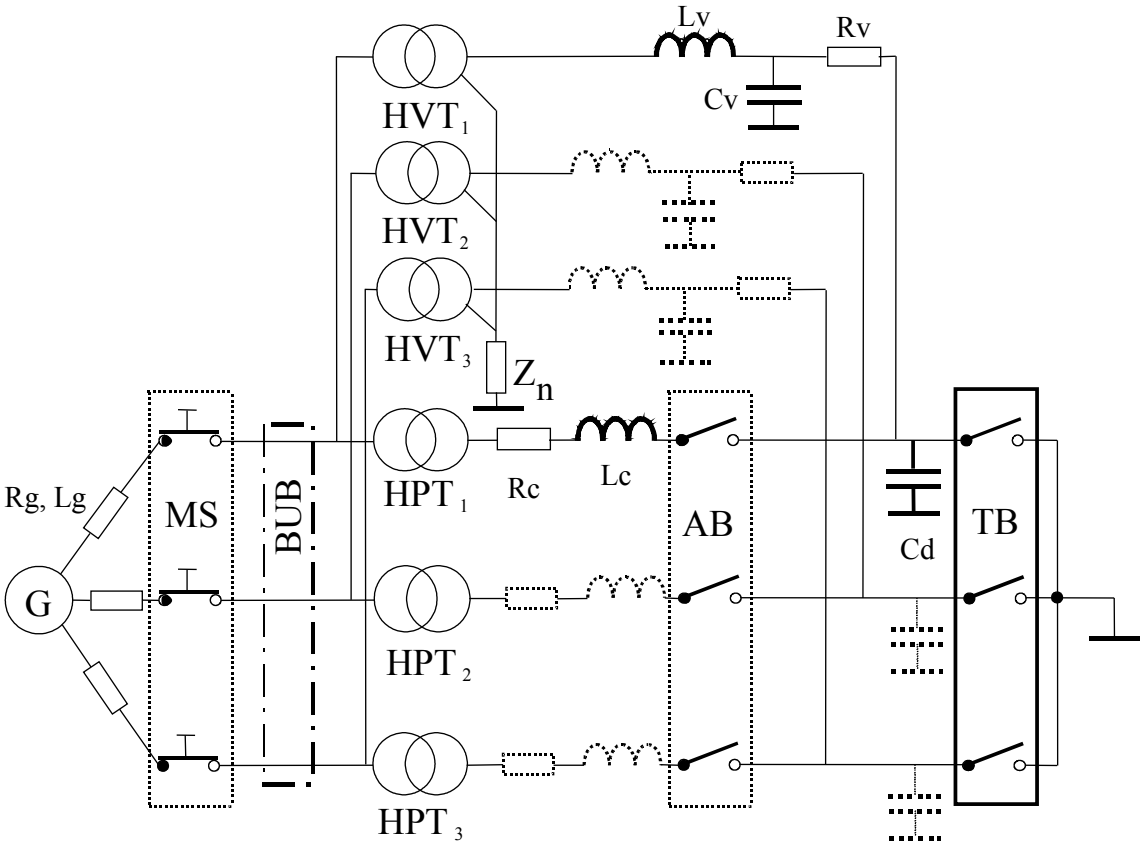

Fig. 5.1 Three-phase Skeats test circuit.

This test circuit will now be dimensioned to test a 245kV/40kA/50Hz 3PCB.

The High Voltage Circuit is a parallel current injection circuit: High Voltage Circuit is connected in parallel to the High Current Circuit during the high current phase.

This introduces small phase shifts between the current of the High Current circuit and the current from the High Voltage circuit, causing the test breaker (TB) to interrupt the current later than the auxiliary breaker (AB).

The current from the High Current supply is:

$$I_c = \frac{V_c}{R_c + jX_c} \cdot e^{j0} = \frac{V_c}{\sqrt{R_c{}^2 + X_c{}^2}} \cdot e^{j\varphi c} \qquad \text{with; } \varphi_c = \arccos \frac{1}{\sqrt{1+(X_c/R_c)^2}}$$

The High Voltage current is:

$$I_v = \frac{V_v}{R_v + jX_v} \cdot e^{j0} = \frac{V_v}{\sqrt{R_v{}^2 + X_v{}^2}} \cdot e^{j\varphi v} \qquad \text{with; } \varphi_v = \arccos \frac{1}{\sqrt{1+(X_v/R_v)^2}}$$

In order to have a realistic dielectric stress, both phase shifts φ_c and φ_v must be equal. To make the AB clear just before the TB interrupts, the phase shift in the high current circuit must be slightly smaller than the phase shift in the high voltage circuit: $\varphi_c < \varphi_v$.

This means that the ratio X_c/R_c must be slightly lower than the ratio X_v/R_v.

The dielectric test circuit with *symmetrical currents* will be analyzed first and then the circuit for *asymmetrical currents* will be dimensioned.

In the Chapter 4 it was calculated that the TRV in a (245kV) Radial Overhead Line Type Network can have the following parameters:

- a steepness of about S_1 = 6.0 kV/μs,
- a time-delay of about t_d = 7 μsec,
- a first peak-factor of at least $\sigma \geq 1.0$,
- a time to first peak within $t_1 \leq 50$ μsec,
- a peak factor of $\gamma \geq 1.50$,
- a time to peak within $t_c \leq 500$ μsec.

And from IEC we know:

The First Pole to Clear Factor for voltages of 245kV and higher is taken to be 1.3.

For this voltage rating the circuit parameters are derived for a symmetrical current and an asymmetrical current.

5.4.1.2.The symmetrical dielectric part test

- The supply circuit:

  The generators have a nominal voltage of V_n = 17,5 kV.

- The single phase high power transformers (HPTs):

  Voltage-ratio: n = (17.5/√3)/(36/√3), S_s = 200 MVA, u_k = 20%, I_{mag} = 0.5 %, P_k = 1200 kW, P_0 = 300 kW, F_n(17,5) = 80 kHz, F_n(36) = 50 kHz

  The High Power Transformers are ynYN connected.

  This results in the following data (V_1 = 17,5/√3 kV);

$n = V_2/V_1 = 2.057$ with V_1 primary voltage and V_2 secondary voltage
$Z_k = u_k*(V_1^2/S_s) = 0.1020833\ \Omega$,
$R_k = P_k*(V_1^2/S_s^2) = 3.0625\ m\Omega \rightarrow X_k = \sqrt{(Z_k^2 - R_k^2)} = 0.1020373\ \Omega$
$L_k = 0.3248$ mH
$R_m = V_1^2/P_0 = 340\ \Omega$

$C_L = \omega/(4\pi^2 F_n^2.X_k) = 12.18$ nF ; C_L is neglected since it has no influence on the TRV across the TB.

- current limiting reactor L_s:

The current limiting reactor L_s is used to tune the current for the high current phase.

- The high voltage transformer (HVT) is three-phase:

Voltage-ratio: $n = (17.5/\sqrt{3})/(245/\sqrt{3})$, S = 200 MVA, u_k = 20%, I_{mag} = 0.5 %, P_k = 1000 kW, P_0 = 400 kW, F_n (17,5) = 80 kHz, F_n(245) = 4 kHz

The HVT is ynYN connected; at the LV side solidly earthed and on the HV side earthed through a Neutral Impedance Z_n.

This results in the following data ($V_1 = 17.5/\sqrt{3}$ kV);

$n = V_2/V_1 = 14$ with V_1 primary voltage and V_2 secondary voltage
$Z_k = u_k*(V_1^2/S) = 0.30625\ \Omega$,
$R_k = P_k*(V_1^2/S^2) = 0.00766\ \Omega \rightarrow X_k = \sqrt{(Z_k^2 - R_k^2)} = 0.30615\ \Omega$
$L_k = 0.9745$ mH
$R_m = V_1^2/P_0 = 765.6\ \Omega$

$C_L = \omega/(4\pi^2 F_n^2.X_k) = 4.06$ nF, $C_H = 8.286$ nF

- The value of the Neutral Impedance X_n (Z_n):

The Neutral Impedance must be such that a First Pole to Clear Factor of 1.3 is achieved. This is done by:

$FPCF = 3k/(1+2k) = 1.3$ with $k = X_0/X_1 \rightarrow k = 1.3/0.4 = 3.25$ and,

$X_0 = 3.25*X_1$ with X_1 the sum of all positive sequence impedances and X_0 the sum of all zero sequence impedances plus $3*X_n$.

$3X_n + (X_k + X_v) = 3.25*(X_k + X_v) \rightarrow X_n = (3/4)*(X_k + X_v)$

- The high voltage tuning Network (L_v, C_v):

Since there is a practical maximum to the value of an air core inductance with little natural capacitance in relation to the maximum current that can flow through it, the first peak reactance (L_v) and the high voltage transformers have to be chosen such that the first-

peak value is 1.

This implicates that L_t and L_v must be of the same order of magnitude; therefore the HVT will be (much) bigger than is in fact necessary to produce the required TRV peak and subsequent RV.

A practical value for an air core reactor used in KEMA's High Power Lab is 160 mH with a Q factor of 25.
This reactor can carry currents up to 3000 A_{peak}, has a capacitance to earth of about 200 – 350 pF and can withstand voltages with a maximum of 1000 kV_{peak}.

For the circuit dimensioning we will assume a value of L_v = 200 mH carrying approximately a current of 1500 A_{peak}.

The tuning capacitance, for an oscillation of 8 kHz, becomes:

$C_v = \omega/(4\pi^2 F_n^2 . X_v) = 1.82$ nF

- The delay capacitance (C_d):

The delay capacitance fixes the delay time t_d:

$t_d = C_d . \sqrt{(L_v/C_v)}$.

- The 3PCB model (as explained in Chapter 3):

To test whether the dielectric test circuits do not stress the 3PCB or TB in the thermal mode, one pole of the 3PCB has to be modeled by the Urbanek arc model with parameters:

ϑ = 7.8 μs, P_0 = 53 kW, u_d = 200 kV and e = 500 V

The other two poles are modeled by ideal switches.

With the model incorporated in a transient program, the thermal severity of that particular pole for the dielectric test can be quantified by calculating Epa.

The same parameters will be used for the 'SLF' part test circuit (see section 5.4.2.1), making it possible to make an Epa comparison.

A bus section is not required since this introduces an extra delay capacitance which is taken into consideration.

For laboratory tests, however, a bus section is necessary if the TB has no separation between the interrupter compartments and the bussection. This requirement gives the test breaker (3PCB) an environment as realistic as possible, because in the extra space 'hot debris' can accumulate during tests.

- The resistors R_c and R_v for the phase correction:

Although R_c carries the short circuit current its value is rather low, of the order of 30 mΩ and the heat dissipation during testing remains within limits.

R_v is of the order of 10 to 20 Ω and has to dissipate the heat produced by the approximately 1 kA_{rms} it carries.

Because of the inter-phase magnetic coupling, through the three-phase HVT and the neutral impedance Z_n, the values for R_c and R_v differ for each pole.

Optimization of the phase shift between the high current circuit and the high voltage circuit is found to be rather tedious and experience shows that it is impossible to get values lower than approx. 700 microseconds for one pole at least.
Two poles can be tuned within a few μsec but the third pole cannot be set under 700 μsec.

Since dielectric recovery is dependent on the di/dt before interruption /12/, the issue that we cannot get the phase angle difference under 700 μsec is in fact a relaxation for this pole for the dielectric part test with symmetrical current.

(For the dielectric part test with an asymmetrical current this would be no problem since that test is meant specifically for testing the dielectric withstand capability in the TRV peak and recovery voltage region.)

A solution for this problem would be to use three single-phase Transformers for the high voltage circuit as well.
This would eliminate inter-phase magnetic coupling and makes independent tuning for all three phases easier.

However, since tuning is already very delicate for ideal circuit breakers installed, it is going to be merely impossible with actual circuit breakers installed.

This can be understood in terms of arc resistance.

Two arcs in series, with their respective nonlinear arc resistance varying from 0.1 Ω in the high current phase till 100 Ω around current zero, being part of the high current circuit, these resistances change the ratio X_c/R_c, with R_c in the order of 10 mΩ, even more than one arc influences the ratio X_v/R_v in the high voltage circuit, when R_v is in the order of 10 Ω.

But even if we could make a correction for this when making the circuit calculations, actual arcs have a statistical behaviour and therefore do not have the same arc resistance from one test to the next. *This makes tuning impossible*.

Conclusion.

So the three-phase dielectric recovery test with symmetrical currents can in practice NOT be done with the proposed three-phase Skeats scheme.

The dielectric test with an asymmetrical current supply is different.

Since it is in particular the AC recovery voltage which causes a dielectric breakdown in the large volume of 'hot' debris after fault interruption, the proposed test circuit – adjusted to supply the required asymmetrical currents - is very suitable for testing this type of fault.

The phase shifts caused by breaker arcs in the tuned circuit are of the order of one to two milliseconds, which has no influence on the TRV peak and recovery voltage as long as the first and other pole to clear factors are correct.

Let us return to the problem of a dielectric test with symmetrical current supply.

The dielectric test with symmetrical current supply must be carried out in a scheme using an injection circuit since this is the only way to keep control on the TRV buildup.

A Transformer scheme is preferable for two reasons:
1. Such a scheme is already used for the asymmetrical dielectric test, so in principle equipment is available.
2. The use of a charged capacitor and some kind of injection method like current or voltage injection (one injection circuit per pole), would generate 'AC' recovery voltages with a decay.

But a Transformer scheme has also disadvantages:
1. In order to achieve the required pole to clear factors for the TRV peak regime, one has to use three separate single-phase transformers or three single-phase transformers with a very large range on the tapchanger.
2. As a consequence the recovery voltages are not what they should be, but they are too high for the first and second poles to clear which can overstress the test breaker.
3. One has to use three injection gaps in order to make things work, an amount not automatically available at a test station.

Another scheme that comes in the picture is the charged capacitor voltage injection scheme. It has the following advantages:
1. Although one needs three independent capacitor banks and injection gaps, the capacitor banks can remain small.
2. The operation and dimensioning of the circuit is commonly known and in operation in many High Power Labs.

This scheme has the disadvantage that the DC-supply generates an 'AC' recovery voltage with a decaying amplitude and understresses the three-phase test breaker in the important dielectric withstand interval.

But since essentially the symmetrical dielectric test has to cover only the TRV region, we could shorten the recovery interval to a few milliseconds after the last pole has interrupted.
The complete recovery voltage interval will be covered by the dielectric part test with asymmetrical current supply.

If a three-phase injection scheme becomes too complicated one could use a single-phase scheme /36/ with three-phase current supply as a good replacement and rotate poles during the testing to cover all phases.

This brings back the number of injection circuits to one and that is available at most test stations /36,44,b,u/.

Although on the face of it single-phase testing seems a relaxation, the dielectric recovery phase is a phenomenon between the opening contacts of a 3PCB pole only and does not play a dominant role between phases.

Between phases it is better to speak of dielectric degradation after an interruption which influences the dielectric withstand capability and this degradation is neatly tested by the Skeats scheme with asymmetrical current

supply (see section 5.4.1.3).

Of course, in order to test with a correct dielectric severity, the dielectric symmetrical tests have to be carried out with a 1-cos or TRF TRV waveform with its characteristic slow start and (very) low thermal severity, but steep dv/dt as occurs in Radial Overhead Line Type Networks (ROLTNs) (Chapter 4).

5.4.1.3.The dielectric part test with asymmetrical current supply

For this test a test circuit as shown in Figure 5.1 can be used.
The make switch (MS) is used to produce the asymmetrical currents.

This type of circuit can be named a 'modified Skeats' and has been highlighted as suitable for testing the dielectric failure modes if the current zero region (thermal failure mode) is of no particular interest or is not considered as a failure mode for a specific extinguishing medium: vacuum breaker /35/.

If an injection circuit is used, one would encounter difficulties, in particular for asymmetrical current tests in providing the 'correct' TRV peak and AC recovery voltages as can be read in /34/.

To produce an asymmetrical current for each pole, the make switch must be triggered independently /41/.

Since we want to create an asymmetrical current decaying with a time constant of τ = 100 msec, we must lay out both the high current circuit and the high voltage circuit in such a way that τ = 100 msec., which corresponds with X/R ≈ 31.

In this case the phase shift in the high current circuit must also be slightly smaller than the phase shift in the high voltage circuit: $\varphi_c < \varphi_v$.

The nonlinear arc resistances of the AB and the TB destroy this balance in such a way that φ_c is always smaller than φ_v and that the time constant of the supply circuit is less than 100 msec.

If we want to take this effect into consideration we can increase both X_c/R_c and X_v/R_v more than required.
To reduce the percentage of influence of the arc resistance in the high current circuit, one can increase the inherently present R_c by using a high power transformer with high copper losses.

The fact that because of the statistical behaviour of the AB and the TB the phase angles can never be tuned such that they are equal in consecutive tests, is more acceptable since with this part test we mainly aim to test the TRV peak and recovery Voltage region, in other words: dielectric withstand capability.

The only requirement that must be met is that the actual phase angles are such that the AB interrupts before the TB does.

It requires adequate timing of the make switches to achieve a 50% DC component at the instant a pole interrupts.
The moment of closing for the MS must be *just before* the generator voltage has risen to 50% of its peak value, i.e. 30 Electrical Degrees (or 3.33 msec. at 50 Hz) after a voltage zero has passed. It is *just before* instead

of *exactly at* to correct for damping.

To see to the fact that the interruptions take place after a major loop only because the maximum amount of energy is by then dissipated in the arc, we have to apply arc reignition circuits (ARCs).

Another way to create a 50% DC component in the current at the instant of interruption is to close the make switches at voltage maximum and take care that current interruption occurs about t = 100*ln2 = 70 milliseconds later.

Simulation of this part test circuit, tuned for a 245kV/40kA/50Hz 3PCB, calculated for ideal breakers, results in the following currents and transient and recovery voltages (Figures 5.2, 5.3 & 5.4 respectively);

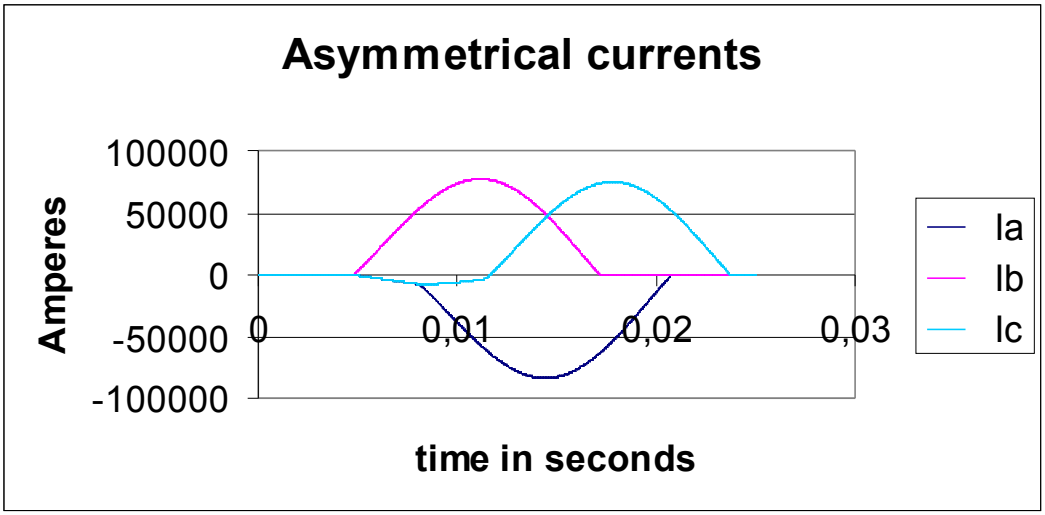

Fig. 5.2 Three-phase asymmetrical supply current through the TB

The asymmetry was created by closing the make switches 'just' before the source voltage reached 50% of its value.

Also one can see that the arc reignition circuits are needed for at least one pole.

In order to be able to control the TB poles close to their maximum arcing time, more than one arc reignition circuit (ARCs) per pole is required. Care must be taken that the last loop is a major loop, otherwise the dielectric stress on that pole is considerably reduced.

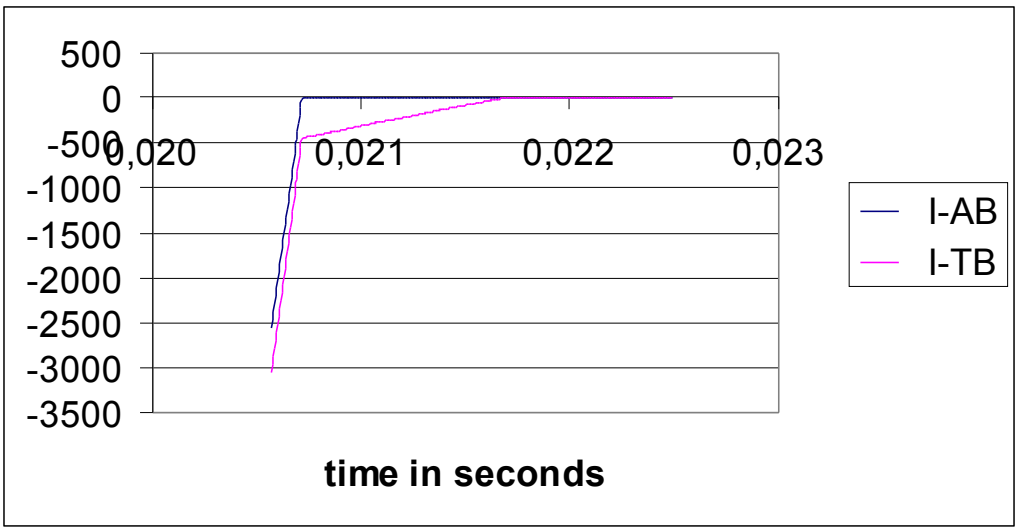

Fig. 5.3 Time difference in interruption between AB and TB for the part test with asymmetrical current supply

In Figure 5.3 we see that the phase difference between the interruption of the AB and the TB is about 1 millisecond on this particular pole.

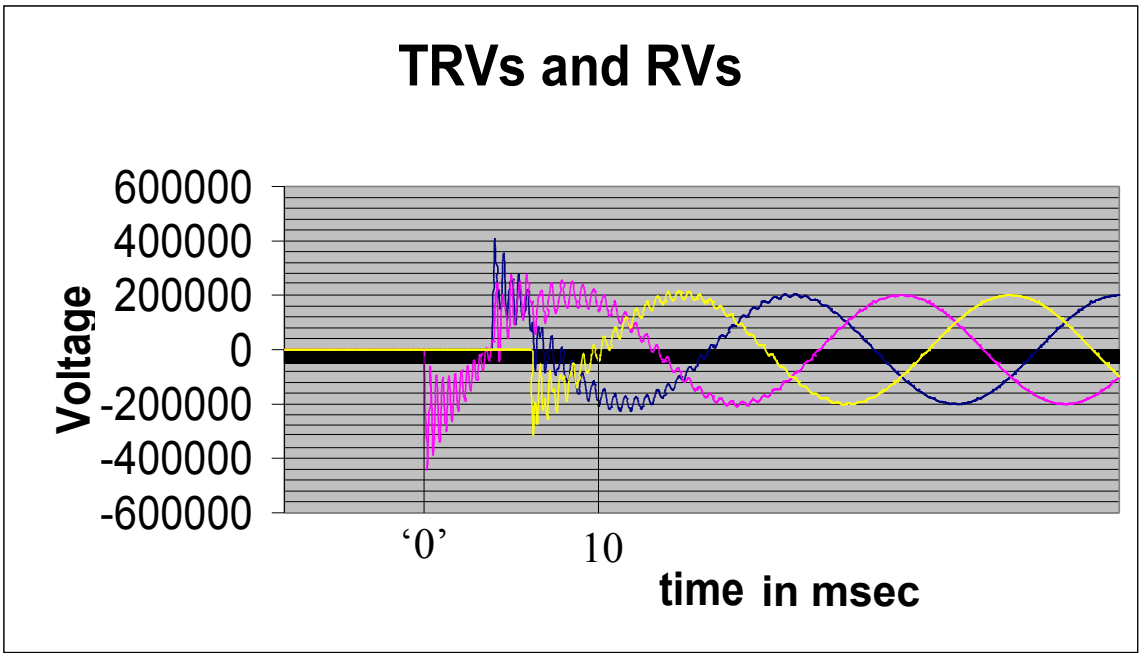

Fig. 5.4 Transient and Recovery Voltages for the part test with asymmetrical current supply

In fig. 5.4 we see that the first, second and third poles to clear factors are automatically correct and that the recovery voltages are correct as well, this means that the test breaker is not overstressed.

The *four* parameter values for the first pole to clear, being pole B, TRV are:

FPCF = 1.3, u_c = 446 kV, t_c = 261 µs, u_1 = 214 kV, t_1 = 93 µs, S_1 = 2.3 kV/µs, t_d = 10 µs, σ = 1.07 and γ = 1.71.

This is too weak on dv/dt, because the di/dt at interruption is lower than

in an optimally tuned symmetrical situation that was used for the occasion.

We can correct the dv/dt by increasing the 'natural' frequency of the current limiting reactor in the high voltage circuit by a factor 3 by means of reducing the externally added capacitance by a factor 9 (It was set to 8kHz corresponding with 1.8 nF).
In a practical circuit this is possible because the reactor has a stray capacitance of approximately 200 to 300 pF.

The Skeats test circuit with adjusted TRV-network does not stress the test breaker in the thermal region as can be seen by an enlarged part of the adjusted TRV (to achieve the required RRRV) of the first pole to clear;

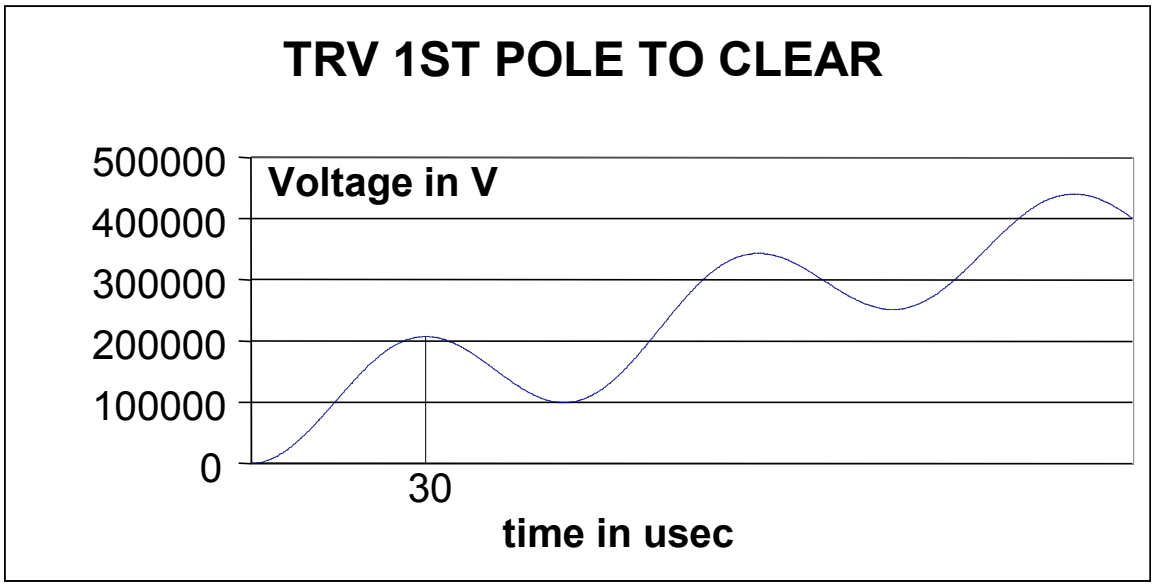

Fig. 5.5 Enlarged TRV for the adjusted 1st pole to clear interruption

The 'flat start' of the TRV caused by the delay capacitance shows up clearly.

Its *four* parameters are:

FPCF = 1.3, u_c = 440 kV, t_c = 142 μs, u_1 = 207 kV, t_1 = 30 μs,
S_1 = 6.9 kV/μs, t_d = 6.5 μs, σ = 1.03 and γ = 1.67.

A thermal stress or Epa analysis, with the circuit breaker model as previously defined inserted in the transient program results in
an Epa = 0 Ws, because of the very low di/dt before interruption and the 'slow' dv/dt of the TRV.

The thermal severity of the test is therefore absolutely minimal and this shows us that a breaker interrupts the current without a thermal reignition and is only tested on its dielectric characteristics.

With the above example we have indicated that, within the framework of the theory, a 3PCB can be tested for its dielectric failure modes by means of two part tests as related to TD4 and TD5.

Another advantage of the proposed Skeats circuit is that, with modification, it can be used successfully for synthetic make tests also /37,42,43/.

5.4.2The thermal part test

To test the thermal failure mode we propose to combine a high current phase with a symmetrical 90% current, because it results in the highest di/dt, in combination with a SLF TRV.
The arcing times must be set such that a minimum arcing time for the first pole to clear and a near-maximum arcing time for the last pole to clear /7/ are achieved.

The above requirements are met by a simple SLF-TRV-circuit in a common direct test circuit because the crest value of the TRV can reach any value as long as the TRV has a dv/dt as straight as possible during the post arc current.

The SLF-TRV must have a very small time delay in correspondence with the current IEC-60056 delay times for ITRV and SLF duties, in order to be in accordance with actual network conditions caused by always present natural capacitances.

The SLF-TRV may deviate slightly from the straight ramp (as for the ideal SLF), not more than for instance 10% as long as the Epa figure is not significantly reduced.

Of course care must be taken that the breaker is tested correctly for what is named the n*on-equilibrium-phase* /4,24/.

This phase occurs during and one or two microseconds after the thermal phase and is characterized by a higher average velocity of the electrons than the heavier particles of the extinguishing arc column.
If the electrons are accelerated in a strong enough electric field a dielectric breakdown can take place.

Cliteur shows that this effect is caused by electron attachment /39/.
In his thesis he shows that non-LTE (Local Thermal Equilibrium) calculations give rise to higher electron density levels (in the first few microseconds after interruption) as compared to LTE calculations. He then shows this effect to be multiplied by the presence of an electric field.

So, this phenomenon is likely to occur when a breaker is tested for its thermal behaviour in a SLF test and successfully passes the thermal region, but fails the test in the early dielectric regime because of the very steep rise in voltage, as is for instance clearly shown in a post-arc current recorded in /25/.

Therefore the 'SLF'-TRV must reach a high enough voltage level as fast as possible, particularly for the first pole to clear, and must have a first-peak factor k of at least 2.4 to 2.7 (see Chapter 4 section 4.4.1.3. and /26/).

From the discussion around Epa we learned that the Short Line Fault is more severe than the ITRV and therefore the Epa produced by our thermal test must equal the (average) Epa produced by currently defined IEC SLF tests.

In Chapter 2 case F we deduced that a combined test: SLF and ITRV, is even more severe. So, to cope with actual system stresses, we could add an ITRV

circuit also.

And next to equal thermal stress, the generated 'SLF'-TRV must reach a sufficiently high voltage level, which is clearly higher than the currently defined SLF peak factors (k = 1.6), in order to correctly test the 'non-equilibrium-phase'.

As we discussed in chapter 4 section 4.4.1.3, for a three-phase SLF it is the first pole to clear which has the most severe duty.

If we want to simulate this behaviour in a 3PTM, we have to make use of different SLF circuits in each phase, but then the use of arc reignition circuits is inevitable to control which pole clears first.

In the case that we do not want to use arc reignition circuits because the extra controls complicate testing considerable, we can make use of three identical lumped RLC-circuits, one in each phase, to generate a SLF TRV. The (average) Epa value of these RLC-circuits should be made equal to the Epa value of the first pole to clear in a practical network (equivalent to IEC 450 Ω requirement).

With such a circuit layout it does not matter which pole comes first, as it will always be stressed by the correct equivalent stress, as would happen in a practical SLF situation.

Interaction between poles can only have an electro-magnetic origin and to test this a GIS-bus of some length is required, as we concluded in the chapter 3.
If the SLF test is performed without the GIS-bus, electro-magnetic interaction is virtually absent and the test will be more severe than in practice since the capacitances of the bus and the short runs of cables reduce the SLF duty considerably as we considered in chapter 4 section 4.4.1.2.

Therefore the SLF or thermal part test consists of three independent uncoupled RLC-circuits in addition to a direct test circuit which produces the required 90% symmetrical short circuit current, without bus and no cables connected to the test breaker.

The idea to make use of a simple ramp voltage to test thermal behaviour, instead of a SLF saw-tooth shaped wave, has been suggested before and has become common practice for development tests, as can be read in /25/.

Unlike dielectric tests, it is not necessary to rotate the SLF test to make that every pole is the 1st, 2nd or 3rd pole to clear, even in the case that the 3PCB has an asymmetrical geometry, because the thermal and early dielectric stresses are taking place between breaker contacts.

Only when the interrupters themselves are not identical or the mechanism exerts unequal force or pressure, phase rotation during tests becomes necessary.
In that case the the most practical procedure is to make use of arc reignition circuits.

5.4.2.1.The operation of the SLF test circuit

As an example we take a 245kV/40kA/50Hz 3PCB to be tested for its interrupting capabilities.

Since the first pole to clear is only important for the TRV peak regime and does not effect the thermal or early dielectric intervals we consider the neutral impedance to be zero.

The circuit we want to use is shown in Figure 5.6.

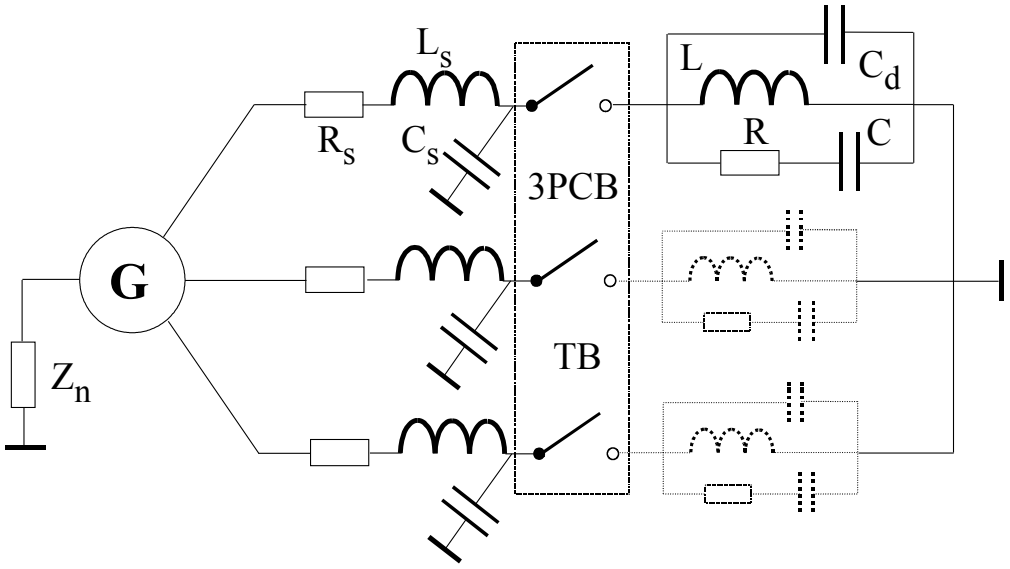

Fig. 5.6 Three-phase Short Line Fault test circuit.

It is a three-phase direct test circuit with the artificial line consisting of identical lumped RLC circuits, in each phase.

The values for R, L and C are chosen such that the RLC circuit generates the ramp of the IEC SLF, but with a higher peak factor:
$Z = 450\ \Omega$, RRRV = 0.2*0.9*40 = 7.2 kV/μsec, t_d = 0.5 μsec and a peak-factor k = 2.4 complying with the analysis in Chapter 4.

Since the RLC circuit has an inherent peak factor k_{eff} of less than two it is necessary to adjust L_s, L and the generator voltage to obtain the required first-peak voltage.

First the situation as it is in practice is analysed:

$V_m = (\sqrt{2}/\sqrt{3})V_n$ = 200 kV, $V_0 = 0.1*V_m$ = 20 kV -> V_p = 2.4*20 = 48 kV

t_L = 48 / (0.2*0.9*40) = 6.7 μsec, $di/dt = \omega\hat{I}$ = 16.0 A/μs.

Because the generator voltage should be as low as possible, the largest inductance value will serve as artificial line (L) and the smallest inductance value as current limiting source inductance (L_s).

If we assume the inherent peak-factor of the RLC-circuit to be $k_{eff} \approx 1.5$ the generator voltage will be:

$V'_0 = 0.9*V_g = V_p/k_{eff}$ -> $V_g = V_p/(0.9*k_{eff})$ = 35.6 kV

The line inductance L and the current limiting source inductance L_s are:

$X_L = (V_g/\sqrt{2})/40$ = 0.629 Ω -> L = 2.0 mH -> L_s = (0.1/0.9)*L = 0.222 mH

For a short circuit generator the source resistance is:

$X_T/R_s = (X_L + X_s)/R_s = 15 \rightarrow R_s = 4.7\ m\Omega$

The value of the lumped capacitance C is:

$T_L = 2\pi/\omega_L = 2*t_L \rightarrow 2\pi\sqrt{(LC)} = 2*t_L \rightarrow$

$C = (t_L^2/\pi^2)/L = 2.27\ nF$

The resistance R must equal the characteristic line impedance R = 450 Ω.

The delay capacitance has the value: $C_d = t_d/R = 1.1\ nF$

The source capacitance C_s should have such a value that it results in a relatively low frequency response on the source side. In most cases a value of 1 μF is sufficient.

If we calculate the transient response of this circuit but without the delay capacitance in the transient program X-trans with a three-phase ideal switch as circuit breaker, the results for the first pole to clear are:

$V_p = 48.7\ kV,\ t_L = 5.7\ \mu sec \rightarrow RRRV' = 8.5\ kV/\mu s$
and
$di/dt = 15.8\ A/\mu s$

The delay capacitance C_d causes a higher peak voltage V_p because of the Ferranti effect.

In the case of a circuit with delay capacitance C_d and a set of parameters based on $k_{eff} = 1.65$, the results for the transient calculation for the first pole to clear are:

$V_p = 48732\ V,\ t_L = 7.2\ \mu sec,\ t_d = 0.6\ \mu sec \rightarrow RRRV' = 7.4\ kV/\mu s$
and
$di/dt = 16.0\ A/\mu s$

For the second pole to clear the results are:

$V_p = 48653\ V,\ t_L = 7.3\ \mu sec,\ t_d = 0.5\ \mu sec \rightarrow RRRV' = 7.2\ kV/\mu s$
and
$di/dt = 16.0\ A/\mu s$

For the last pole to clear:

$V_p = 48694\ V,\ t_L = 7.0\ \mu sec,\ t_d = 0.8\ \mu sec \rightarrow RRRV' = 7.9\ kV/\mu s$
and
$di/dt = 16.0\ A/\mu s$

These values indicate that all poles are more or less stressed as the first pole to clear of a 3PCB operating in an actual system interrupting a three-phase SLF.

This is not much of a problem since interphase interaction is negligible for the thermal interruption mode, since the breaker is tested without an additional busbar connected to it.

The early dielectric mode, during the post arc current and the first few microseconds after it has ceased, is also tested equally for each pole. This is more severe than this failure mode would be stressed in a practical SLF interruption in the system.

To verify whether this lumped element RLC circuit stresses a breaker correctly, that is as a SLF fault in the system would stress the breaker, we will now compare Epa values for the Urbanek model tuned to simulate a 245kV/40kA/50Hz SF6 breaker (see section 5.4.1.2) interrupting a 90% three-phase SLF on an untransposed line with a characteristic impedance of 450 Ω. The corresponding overhead line tower configuration and wire diameter are not very realistic but result in the required 450 Ω in the EPRI/EMTP v3.0 program.

This is more accurate than only defining waveforms. In chapter 2 we have learned that defining di/dt before current zero and dv/dt after current zero, as is the practice of IEC, is not enough.
This was already concluded by Rieder and Kuhn in 1961 /38/.

The results for the first pole to clear are shown in table 5.1:

	RLC	SLF	SLFD
Epa	0.0009379 Ws	0.0068291 Ws	0.0025838 Ws

Table 5.1 Epa values for an SLF interruption with the RLC-line, a practical line and a practical line with stray capacitance.

Comparing the RLC and SLF Epa values in table 5.1 we can conclude that this RLC test circuit (k_{eff} = 1.65) does not stress the breaker model in the thermal mode as the power system does.

The reason behind this is that the power system SLF does not have a delay capacitance, but in practice it is there. If we add this capacitance we get the SLFD Epa value.

Comparson of the Epa's of the RLC circuit and this SLFD circuit shows that the arc model is stressed with a more realistic stress.
The difference is caused by the fact that the RLC circuit produces a '1-cos' wave form and the SLFD circuit produces a ramp.
Both Epa's can be made equal by adjusting the delay capacitance in the RLC circuit.
In an actual SLF test circuit this should be done based on average Epa-values for a range of circuit breaker models.

From the calculated wave forms, the initial part of the first pole to clear for an ideal switch and the 3PCB-model both interrupting the 90% SLF is shown in Figure 5.7.

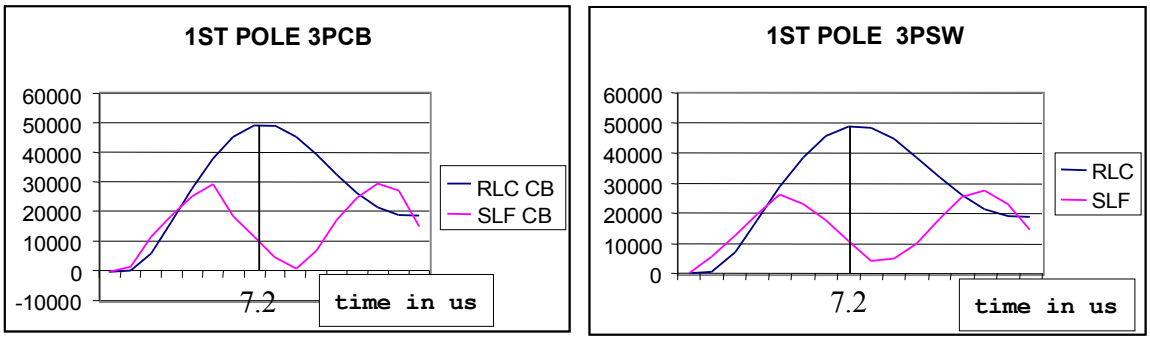

Fig. 5.7 Initial part of the TRV-waveforms for a network SLF oscillation and a RLC circuit.

Figure 5.7 shows that the SLF oscillation without the delay capacitance puts more stress on the breaker model (second plot).

In the first plot, with the Urbanek model inserted, we see that the CB-model clearly influences the SLF wave.

With the above example we have indicated that, within the framework of the theory, a 3PCB can be tested for its thermal and early dielectric failure mode with a very simple three-phase SLF part test.

5.4.3Seamless TRV overlap dielectric and thermal part tests ?

From our previous discussions it will be obvious that mechanical and thermal stresses are tested seamlessly by the 3PTM.

All dielectric failure modes, that is early, recovery and withstand, are tested seamlessly as well. This can be seen in Figure 5.8.

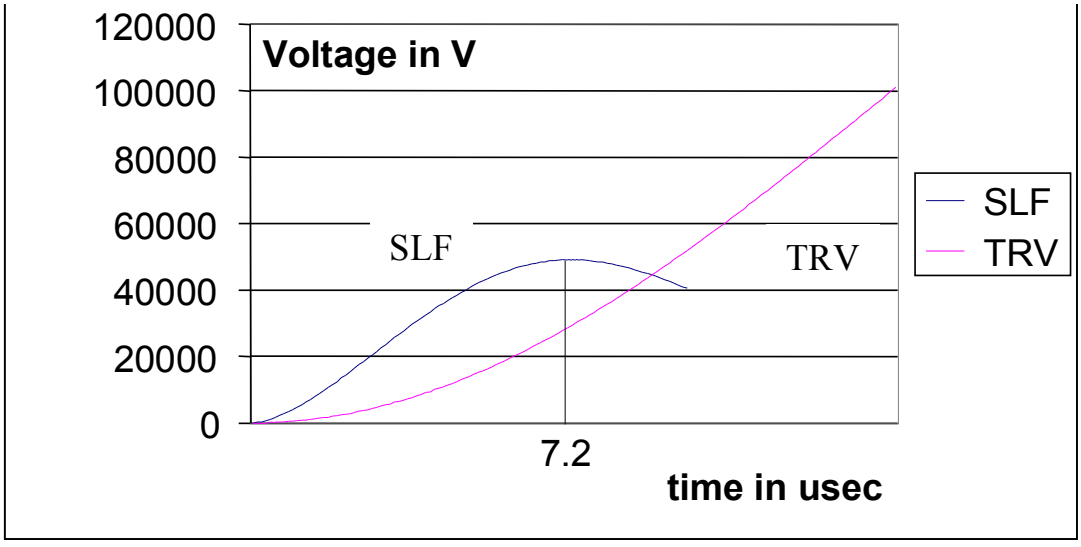

Fig. 5.8 TRV of SLF Test and TRV of (a)symmetrical Dielectric Test.

From this plot one can see that the SLF TRV build-up in the thermal part test covers the lower voltage range of the early dielectric recovery region of a SF6 circuit breaker.
Whereas the TRV build-up in the dielectric part tests covers the voltage range after that, i.e. the dielectric recovery and dielectric withstand region.

5.5 Summary

Instead of the defined IEC test duties for SLF, TD4 and TD5, it is proposed to use *a two-Part Test Procedure (2PTP)* , with again *three* test duties:
1. full three-phase short line fault test,
2. single(/three)-phase dielectric test with symmetrical current supply and
3. full three-phase dielectric test with asymmetrical current supply
for testing three phases in one tank type circuit breakers (3PCBs).

Test Duties 1, 2 and 3 are still necessary to be performed since for self-blast puffer interrupters and rotary-arc interrupters the interrupting capability has a relation with the current to be interrupted /11/.

In the case of the smaller fault currents (TD1, 2 and 3) the self-pressurizing effects of the self-blast design and the nozzle-blocking of puffers or the rotational force causing convection cooling for rotary-arc types are smaller and the breaker has to operate at a different 'operating point'.

These tests can be single-phase since the phenomena involved are restricted to the interrupting pole only.

The proposed two-Part Test Procedure (2PTP) uses a three-phase lumped element test methods (3PTM) to test a 3PCB for its maximum capabilities for the three failure modes:

- Mechanical failures during the high current phase
- Thermal failures during the interaction interval and
- Dielectric breakdown during the dielectric recovery intervals and subsequent dielectric withstand period.

The three-phase test method is based on the assumptions that:

- If the test breaker passes the three-phase Short Line Fault test, it will not fail thermally in any maximum fault-current interruption, and Short Line Fault situation.
- If the test breaker passes both three-phase dielectric duties, it can withstand any transient recovery voltage or recovery voltage in other networks.
- If the test breaker passes both dielectric tests, it is capable of enduring the mechanical stresses from any short circuit currents.

To prove these statements, it is unfortunate that one should perform many comparison tests /33/, as was done by Heroin et al. /27/ in 1966 or Anderson et al. /28/ between 1966 until 1968 to show equivalence between direct and synthetic testing.

This would create a statistical basis for comparison, which could be compared to values, obtained for 'single-phase' circuit breakers.

Instead the numerical analyses and the extensive literature survey have supplied us with the evidence.

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6 CONCLUSION AND RECOMMENDATIONS.

6.1 Conclusion

In this thesis we have shown that three-phase in one enclosure type circuit-breakers (3PCBs) have to be tested in a different way than their 'single-phase' (1PCB) predecessors.

It is shown that it could be inadequate to test 3PCBs by current standards and testing techniques, which are mainly based on 1PCBs.

3PCBs are a real departure from previous circuit breaker developments as inter-phase interaction/insulation or phase-to-tank insulation is stressed in a different and more intense way.

In order to make a distinction between the different types of stresses a circuit breaker is subjected to, we have developed a new tool: Epa.

With the aid of this tool we are able to disentangle the different stresses a circuit breaker is subjected to when interrupting a short circuit current.

We find the usual stress intervals a circuit breaker passes through when interrupting a short circuit current, that is the high current interval, the interaction interval and the dielectric interval.
However, with Epa we are able to put a figure to the most elusive of the three: the interaction interval.

During the interaction interval a circuit breaker is subjected to the so-called thermal stress.

The ability to state that: the thermal stress exerted by a test circuit on a specific circuit breaker is x.yz Ws, opens the door to a whole range of analyses with the outcome that circuit breakers (and 3PCBs in particular) can be tested by a kind of two-part test method.

Due to this kind of two-part test method the three-phase lumped element test method (3PTM) becomes rather simple to devise, apart from the fact that one cannot automatically apply the currently defined dielectric stresses in IEC standards.

These stresses are based on investigations into the nature and form of the Transient Recovery Voltage (TRV) during the 1960s, but present day networks have departed from the networks investigated then.

In an extensive but not very complicated investigation into the nature and form of the TRV a 3PCB will experience in present-day and future networks, it is shown that especially the commonly used overdamped 4-parameter test TRV has to be revised to account for 'new' network characteristics and (three-phase) dielectric circuit breaker weaknesses.

The proposed three-phase lumped element test method (3PTM) is able to cover these 'new' TRVs.

On the one hand it consists of two dielectric tests comparable to IEC TD4 and IEC TD5. One of these tests may be a single-phase synthetic (voltage) injection scheme to test for the dielectric recovery regime, while the

other must be a three-phase 'Skeats' scheme to test for the dielectric withstand regime.

On the other hand a three-phase Short Line Fault (SLF) test is used to test for the thermal weaknesses of a 3PCB and - through a high first peak voltage - for its early dielectric recovery weakness as well.

6.2 Recommendations

Because of obvious restrictions the major part of this research was done with access to a computer only and the wealth of literature written on the subject to assist in the understanding of the behaviour of the electric arc. The results of some practical experiments (KEMA tests) were used as well but several assumptions or short-cuts had to be made.

And although great care was taken as to see to the fact that every assumption could be traced to some practical experiment or experience, the foundations for this thesis may be improved by doing more practical experiments on several occasions.

6.2.1Epa

This tool is based on numerical analyses and therefore additional experiments showing it to be true are very desirable.

Epa stands for Energy-post-arc and is defined as:

$$Epa = \int_0^\infty v_a i_a dt$$

with v_a and i_a being the arc voltage and current respectively in the post-arc regime.

This simple integral turns out to be an excellent measure for arc-circuit-interaction or thermal severity.

To make this plausible one has to realize that during the arc-circuit-interaction interval it is an energy balance that decides whether a circuit breaker will interrupt or fail to do so.

Proving the validity of Epa, however, is quite another matter.

In order to do so, one has to do a large number of tests to filter out arc stochastic behaviour and measure the post-arc current and TRV each time with great accuracy.
This last requirement cannot be fulfilled since, even today, with all our knowledge and (digital) electronic technology, we are quite incapable of measuring the post-arc currents of commercial SF6 circuit breakers in the order of only several tens of milli-amperes or less.

What could be done is to measure post-arc currents in mock circuit breakers such as are used to investigate the behaviour of the SF6 arc.
However, these mock circuit breakers and the test circuits in which they operate are far from identical to commercial breakers and their network environment. So the outcome of such experiments is open to debate.

Another way would be to analyse many more - single phase - test series on fully conditioned circuit breakers in a fully standardized – SLF - test

circuit (like the ones done by KEMA) and each time find the parameters for one or more circuit breaker models based upon the behaviour of the arc up to current zero, i.e. a region in which we feel secure that the measurements are really what they seem to be.

Fig. 6.1 KEMA measuring system to enable CB-modelling and digital testing.

With the model, its parameters and the (simplified) test circuit it is then – for most interruptions – possible to do numerical analyses and find the resulting Epa-series.

These Epa-series could then be compared to other trends in, for instance, the 50% interrupting probability or other indicator, observed when analysing the test series by other means.

A problem with this kind of comparisons is that some measured post-arc current traces do not show the characteristic, apparently unimpeded current around current-zero but a kind of 'delayed' post-arc current.
For this type of interruptions phenomenological arc models have so far been unable to model this current waveform.

6.2.2Network stresses.

Present-day and future networks are departing from the meshed networks of the past.

Therefore, circuit breakers having to operate in modern networks are stressed in a different way than was investigated and standardized in the past.

The most noticeable difference is that TRVs generated when maximum short circuit currents are interrupted, can be of a more or less single-frequency nature and overdamped TRVs are no longer the only types occurring.

This fact, in conjunction with the fact that during the dielectric recovery interval an SF6 circuit breaker is more vulnerable to a TRV of the

'1-cos' form, brings us to the conclusion that: standard 4-parameter TRVs, as are commonly used for circuit breaker testing, should be replaced by Transformer TRVs.

In this thesis we have been able to make this plausible. To prove the fact that TRV wave forms are really changing, a worldwide study into the exact nature of the TRVs in the present-day and future networks would give a more reliable picture.

At least it should be investigated what the natural frequencies of large transformer banks would be, because this is the key parameter for the biggest departure from the networks of the past: the increase in the Rated Rise of Recovery Voltage (RRRV).

In this thesis we have based ourselves on measurements and curves reported in 1970 that could be obsolete as new core-iron materials have been introduced and the capacitances of windings and bushings will have changed as well.

6.2.3Three-phase lumped element test method

The proposed three-phase lumped element test method (3PTM) is new insofar as that the SLF test circuit is based on a common reduced voltage direct test circuit and the usual saw-toothed wave and TRV peak is not generated.

The proof that this is okay is based on Epa and is therefore open to criticism.

It is possible to prove this part test to be valid by doing a large number of single-phase comparison tests in both: a normal SLF test circuit and the simple 'low-voltage' SLF circuit.
A statistical comparison should then give evidence of the validity of the 'low-voltage' SLF test.

Another thing on which the 3PTM is based is that the single-phase dielectric recovery part test is as good as a three-phase dielectric recovery part test would be. To prove this, again, one would have to do a large number of comparison tests on, for instance, a small three-phase breaker (which can still be tested in a direct test circuit) and to repeat these tests in the single-phase dielectric part test. This should then give evidence of the assumed equivalence.

A last thing that could be investigated is the fact that SF6 circuit breakers are more sensitive to transformer TRVs than to currently used (overdamped) 4-parameter TRVs when going through the dielectric recovery stages after interruption.
Although this fact can be deduced from several sources, an experimental basis would be even better.
This basis can be created by doing some tests with an SF6 breaker at the boundaries of its dielectric recovery abilities and subjecting it to both a standard 4-parameter TRV and a transformer TRV.

List of Abbreviations and Symbols.

Abbreviations:

1PCB	'Single' Phase Circuit Breaker
2PTP	Two Part Test Procedure
3PCB	Three-phase Circuit Breaker
3PTM	Three-phase Test Method
AB	Auxiliary Breaker
ABB	Air Blast Breaker
AC	Alternating Current
ARC	Arc Reignition Circuit
ATP	Alternative Transients Program
BB	Backup Breaker
BTF	Breaker Terminal Fault
CB	Circuit Breaker
CESI	Italian High Power Laboratory
Cigre	Conference Internationale des Grands Reseaux Electriques
CT	Current Transformer
CTN	Cable Type Network
DC	Direct Current
EGS	Effectively Earthed System
EHV	Extra High Voltage
EMTP	ElectroMagnetic Transients Program
Epa	Energy post arc
EPIC	Enhanced Parallel Injection Circuit
ETZ	ElektroTechnisches Zeitschrift
FPCF	First Pole to Clear Factor
G	Generator
GCB	Gas Circuit Breaker
GIS	Gas Insulated Substation
HPL	High Power Laboratory
HPT	High Power Transformer
HV	High Voltage
HVT	High Voltage Transformer
IEC	International Electrical Commission
IEE	Institute of Electrical Engineers
IEEE	Institute of Electrical and Electronical Engineers
ITRV	Initial Transient Recovery Voltage
KEMA	Dutch High Power Laboratory
L	Reactor
MOLTN	Meshed Overhead Line Type Network
MS	Make Switch
NEGS	Non Effectively Earthed System
PT	Potential Transformer
RFC	Rate of Fall of Current
ROLTN	Radial Overhead Line Type Network
RRRV	Rated Rise of Recovery Voltage
RV	Recovery Voltage
RWTH	Rheinland Westfaellische Technische Hochschule
SC	Study Committee
SCF	Short Circuit Factor
SF6	Sulfer hexaFluoride
SLF	Short Line Fault
SPCF	Second Pole to Clear Factor
STL	Short-circuit Testing Liaison
STZ	Schweizerische Technische Zeitschrift
TB	Test Breaker
TD	Test Duty
TNA	Transient Network Analyzer
TPCF	Third Pole to Clear Factor
Tr	(Short circuit) Transformer

TRV	Transient Recovery Voltage
T-PAS	Transactions on Power Apparatus and Systems
T-PS	Transactions on Plasma Science
T-PWRD	Transactions on Power Delivery
UHV	Ultra High Voltage
WG	Working Group

Symbols:

cos	cosine
C	Capacitance
dx/dt	derivative of x to time
e	2.718281828
exp	2.718281828
f	frequency in Herz
F	Fahrad
F_n	Natural Frequency
g	Conductance
G	Conductance
i	Current (time dependant)
I	Current (amplitude)
k	(SLF) peak factor
k	X_0/X_1
L	Inductance
ln	natural logarithm
P	Power
π	3.141592654
Q	Heat
R	Resistance
sin	sine
S_1	TRV steepness (RRRV)
t	time
tan	tangent
t_d	delay time (TRV)
T	Temperature
u	gas flow velocity
v	Voltage (time dependant)
V	Voltage (amplitude)
Ws	Watt-seconds (Joule)
X	Reactance
Z	(characteristic) Impedance
Ω	Ohm
ϕ	phase
γ	amplitude factor (TRV)
φ	angle
σ	first peak factor (TRV)
ω	(power) frequency in radians/sec

Numeric indicators:

kA	kilo Ampere
km	kilometer
kV	kilo Volt
kW	kilo Watt
msec	milliseconds
MV	Mega Volt
MVA	Mega Volt Ampere
μsec	microseconds
nWs	nano Wattseconds (Joule)

APPENDIX I

Chapter 2: KEMA datasets (European Project SMT4-CT96-2121).

Test No	S[A/us]	Epa [nWs]	R/I (test)	Pole	tarc[ms]	D/S
11	13,89	26,8	I	A	18,5	S
12	13,9		R	A	18,5	S
13	13,86	23,5	I	A	18,5	S
14	13,9	1270,4	I	A	18,5	S
15	13,9		R	A	18,5	S
16	13,86	57,6	I	A	18,5	S
17	13,88	435,3	I	A	18,5	S
18	13,9		R	A	18,5	S
19	13,87	701,3	I	A	18,5	S
20	13,89	607986	I	A	18,5	S
21	13,92		R	A	18,5	S
22	13,92		R	A	18,5	S
24	6,99	0,36	I	B	18,5	S
25	7,02	1153,8	I	B	18,5	S
26	7,02	0,012	I	B	18,5	S
27	9,78	0,713	I	B	18,5	S
28	9,77	0,023	I	B	18,5	S
29	9,76	1,59	I	B	18,5	S
30	13,9	6,24	I	B	18,5	S
31	13,88	95,46	I	B	18,5	S
32	13,89	67848,9	I	B	18,5	S
33	15,28		R	B	18,5	S
34	15,3	1571,02	I	B	18,5	S
35	15,32		R	B	18,5	S
36	13,86	1,75	I	C	18,5	S
37	13,87	9,14	I	C	18,5	S
38	13,9	14,75	I	C	18,5	S
39	16,66	76,59	I	C	18,5	S
40	16,64	164650	I	C	18,5	S
41	16,68	1713,45	I	C	18,5	S
42	16,74		R	C	18,5	S
43	16,68		R	C	18,5	S
44	13,86	831,34	I	C	18,5	S

Table 1. Epa values for a 123kV SF6 Circuit Breaker

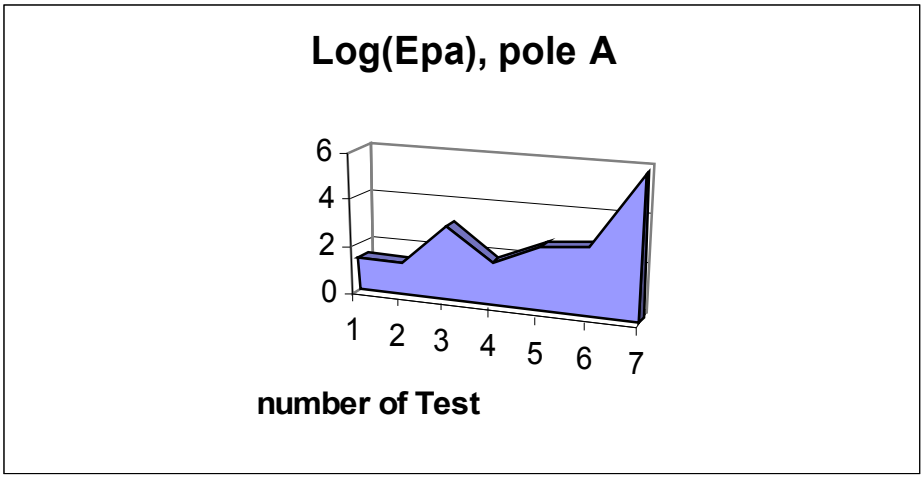


Fig. 123.1

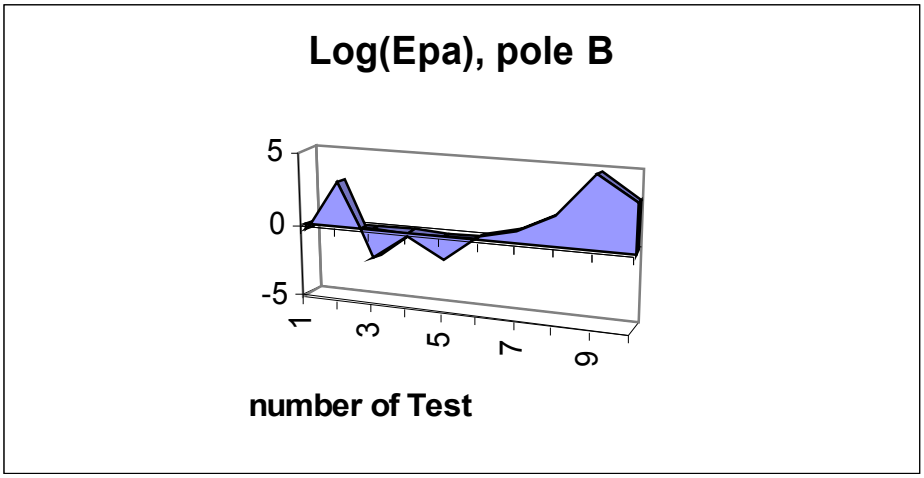


Fig. 123.2

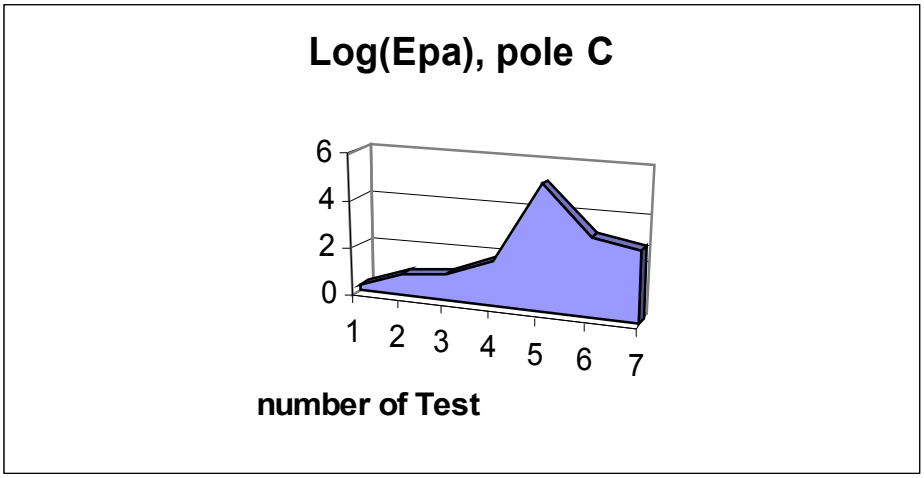


Fig. 123.3

Test No	segment	S[A/us]	R/I (test)	Epa nWs	Epa uWs	pole	tarc[ms]	D/S
				KEMA	TUD			
21	2	10,34	R			A	3,6	D
21	3	10,1	I	142,48	54,629	A	12	D
22	2	14,49	R			A	4,97	D
22	3	14,44	I	14739,8	70,633	A	13,3	D
23	2	13,62	R			A	2,07	D
23	3	13,56	I	80,27	1178,799	A	10,4	D
24	2	13,83	R			A	7,67	D
24	3	13,78	I	305,19	929,924	A	16	D
25	2	13,77	R			A	7,74	D
25	3	13,82	R			A	16,07	D
25	4	13,89	I	143183,7	7332,413	A	24,4	D
26	2	13,76	R			A	7,74	D
26	3	13,78	R			A	16,07	D
26	4	13,82	R			A	24,4	D
27	2	11,56	R			A	7,74	D
27	3	11,52	R			A	16,07	D
27	4	11,54	R			A	24,4	D
28	2	11,88	R			B	7,57	D
28	3	11,78	I	947,4	119,021	B	15,9	D
29	2	11,89	R			B	7,77	D
29	3	11,85	I	1,29	-	B	16,1	D
30	2	11,86	R			B	7,27	D
30	3	11,84	I	218,2	1069,6	B	15,6	D
31	2	11,84	R			B	7,27	D
31	3	11,73	I	375768,4	925,249	B	15,6	D
32	2	11,81	R			B	7,67	D
32	3	11,72	I	11879150	9508,55	B	16	D
33	2	11,79	R			B	6,57	D
33	3	11,78	I	33034,7	6891,25	B	14,9	D
34	2	11,81	R			B	6,57	D
34	3	11,78	R			B	14,9	D
34	4	11,85	R			B	23,23	D
35	2	9,21	R			C	5,67	D
35	3	9,21	I	1,45	ERROR	C	14	D
36	2	9,27	R			C	5,47	D
36	3	9,27	I	0,796	ERROR	C	13,8	D
37	2	9,24	R			C	4,97	D
37	3	9,3	I	0,06	24,98	C	13,3	D
38	2	9,29	R			C	4,67	D
38	3	9,25	I	1761,7	185,46	C	13	D
39	2	9,28	R			C	3,77	D
39	3	9,29	I	17482,7	570,26	C	12,1	D
40	2	9,23	R			C	3,97	D
40	3	9,3	I	321,19	358,52	C	12,3	D
41	2	9,21	R			C	2,97	D
41	3	9,21	I	190,29	529,46	C	11,3	D
42	2	9,23	R			C	3,07	D
42	3	9,24	I	3559,49	3326,29	C	11,4	D
43	2(VZ=0)							
43	3	9,13	I	206,97	-	C	10,1	D
44	2	9,23	R			C	2,27	D
44	3	9,23	I	104,84	1150,75	C	10,6	D

45	2	9,23	R			C	1,4	D
45	3	9,19	R			C	9,8	D
45	4	9,33	I	FAILED	FAILED	C	18,1	D
46	2(VZ=0)							
46	3	9,24	R			C	9,77	D
46	4	9,36	I	4255,48	3475,62	C	18	D
47	2	9,31	R			C	7,94	D
47	3	9,17	R			C	16,27	D
47	4	9,37	I	2325302	8861,67	C	24,6	D
48	2	9,29	R			C	7,94	D
48	3	9,26	R			C	16,27	D
48	4	9,32	R			C	24,6	D

Table 2. Epa values for a 72.5kV circuit breaker.

Note:

Failed means that a thermal reignition occurred,
ERROR means that a numerical problem occurred and
- means that no parameter fit was available.

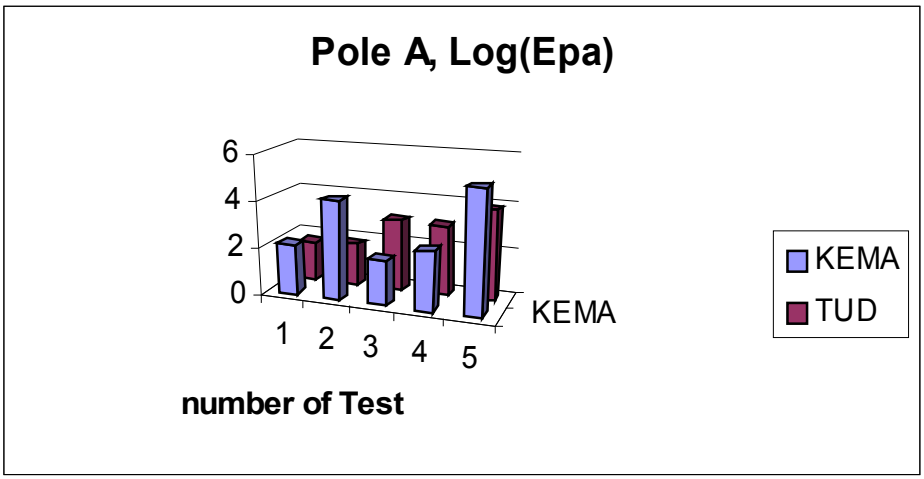


Fig. 72.1 Log(Epa) values, pole A

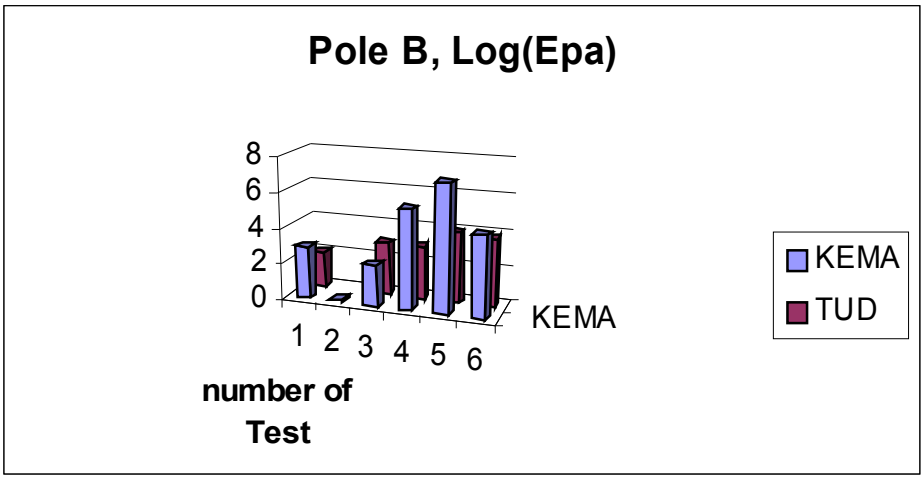


Fig. 72.2 Log(Epa) values, pole B

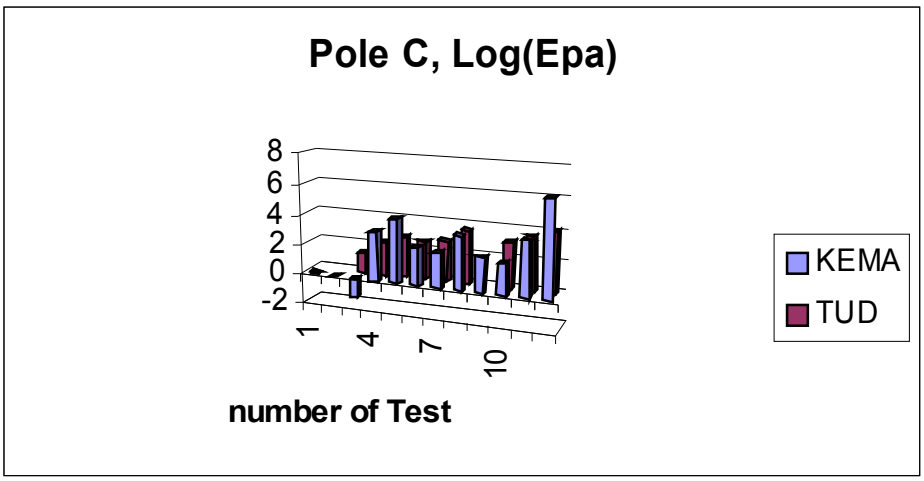


Fig. 72.3 Log(Epa) values, pole C

Test No	segment	S[A/us]	R/I (test)	Epa nWs	pole	tarc[ms]	D/S
3	1	7,75	R		C	3,47	D
3	2	8,19	I	0,18	C	11,8	D
4	1	7,84	R		C	2,77	D
4	2	8,18	I	420,68	C	11,1	D
5	1	14,49	R		C	3,57	D
5	2	14,51	I	1487,93	C	11,9	D
7	2	14,5	I	883353,5	C	9,5	D
8	2	14,49	R		C	7,77	D
8	3	14,47	I	7318,84	C	16,1	D
9	2	14,13	R		C	7,77	D
9	3	14,19	I	2831,64	C	16,1	D
10	2	14,14	I	Failed	C	16,1	D
11	2	14,09	R		C	7,77	D
11	3	14,21	I	368972,3	C	16,1	D
12	2	14	R		C	7,77	D
12	3	14,09	I	40653,37	C	16,1	D
13	2	14,09	R		C	6,67	D
13	3	14,05	I	232325,2	C	15	D
14	2	14,07	R		C	5,57	D
14	3	14,17	I	122685	C	13,9	D
15	2	13,99	R		C	4,67	D
15	3	13,97	I	32,55	C	13	D
16	2	13,94	R		C	3,77	D
16	3	14,05	I	2672,6	C	12,1	D
17	2	0	R		C	2,77	D
17	3	14,25	I	314138,8	C	11,1	D
18	2	13,95	R		C	1,67	D
18	3	14,1	I	30147,93	C	10	D
19	3	14,05	I	1723,86	C	9	D
20	3	14,06	R		C	8,07	D
20	4	14,16	I	1751,32	C	16,4	D
21	3	14,1	I	32403,38	C	8,1	D
22	3	14,02	R		C	7,17	D
22	4	14,09	I	16773,14	C	15,5	D
23	2	14,01	R		C	7,17	D
23	3	14,22	I	592,52	C	15,5	D
24	2	14,07	R		C	6,97	D
24	3	14,05	I	13827,92	C	15,3	D
25	2	14,02	R		C	7,07	D
25	3	14,05	I	181,83	C	15,4	D
26	2	14,13	R		C	7,07	D
26	3	14,12	I	633365,6	C	15,4	D
27	2	14,1	R		C	7,07	D
27	3	14,19	I	147793,6	C	15,4	D
28	2	14,12	R		C	7,17	D
28	3	14,2	I	98,57	C	15,5	D
29	2	14,08	I	Failed	C	7	D
30	2	14,07	R		C	7	D
30	3	13,96	R		C	15,33	D
30	4	13,94	R		C	23,66	D
103	1	10,37	I	1284,19	B	12	S
104	1	13,36	I	163948,4	B	12	S
105	1	13,42	I	118708,8	B	10,9	S

106	1	13,44	I	472252,7	B	10,1	S
107	1	13,44	I	41451,25	B	9,1	S
109	1	13,46	R		B	8,2	S
110	1	13,44	R		B	8,2	S
111	1	13,45	R		B	8,2	S
112	1	13,87	I	3835,68	B	9	S
113	1	13,87	R		B	9	S
114	1	14,31	I	Failed	B	8,9	S
115	1	14,33	R		B	8,9	S
116	1	13,5	I	3937,68	B	16,5	S
117	1	13,37	I	49012,8	B	16,5	S
118	1	13,37	I	236,01	B	16,5	S
119	1	13,48	I	1,13	B	16,5	S
120	1	13,22	I	5200,12	B	16,5	S
121	1	13,15	I	252,88	B	15,4	S
122	1	13,22	I	0,0062	B	14,5	S
123	1	13,21	I	1259,73	B	13,5	S
124	1	13,18	I	69460,39	B	12,6	S
125	1	13,2	I	134,27	B	11,6	S
126	1	13,2	I	880,74	B	10,5	S
127	1	13,2	I	11857,91	B	9,7	S
128	1	13,25	I	34396,2	B	9,7	S
129	1	13,22	I	32760,55	B	8,6	S
130	1	13,25	R		B	7,6	S

Table 3. Epa values for a 145kV puffer SF6 Circuit Breaker.

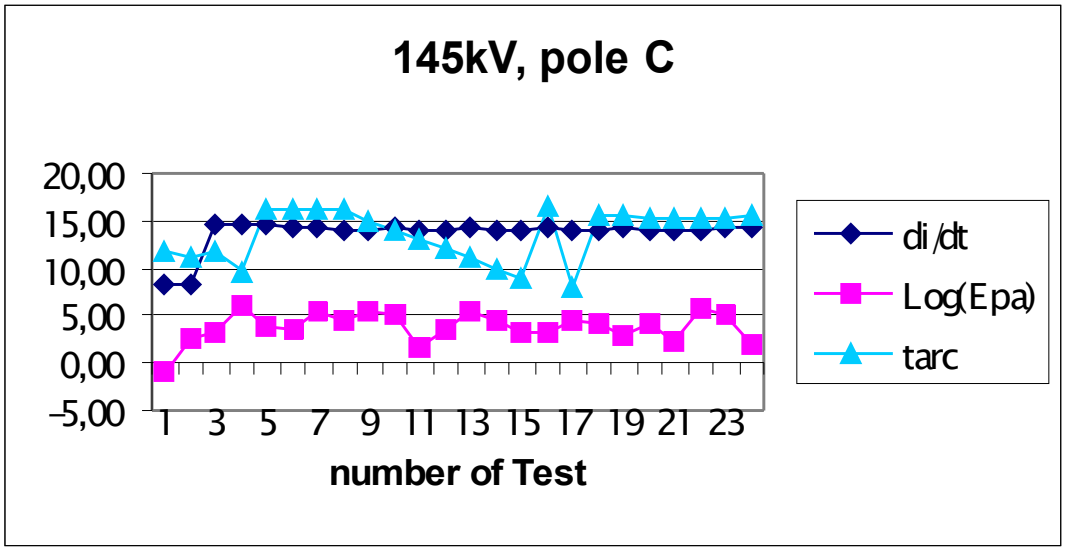


Fig. 145.1, direct SLF-test

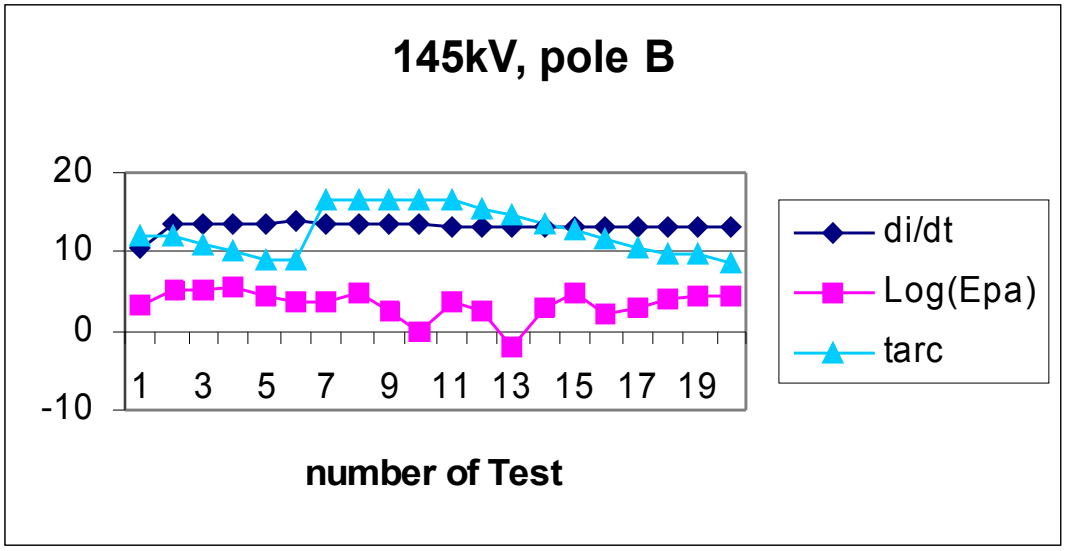


Fig. 145.2, synthetic SLF-test

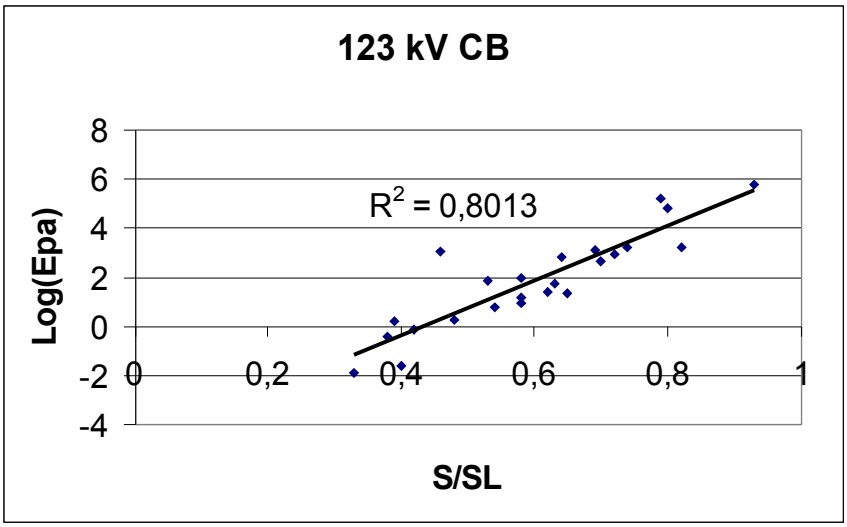


Fig. 123.S

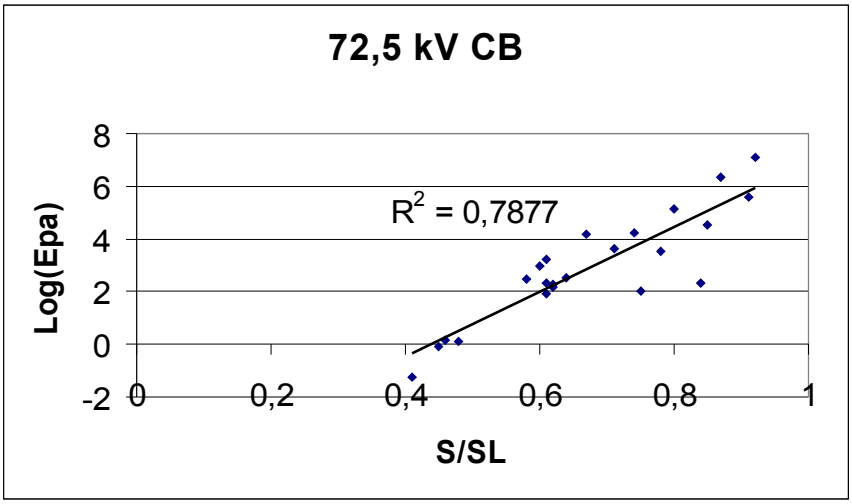


Fig. 72.S

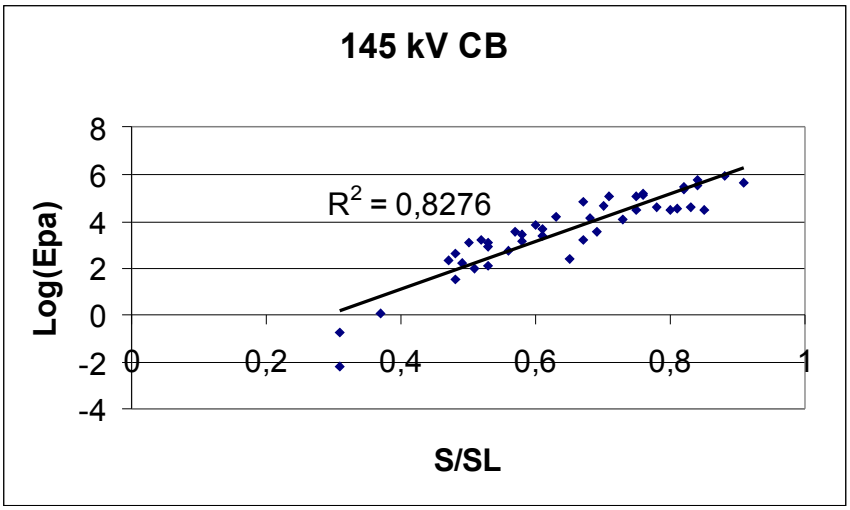
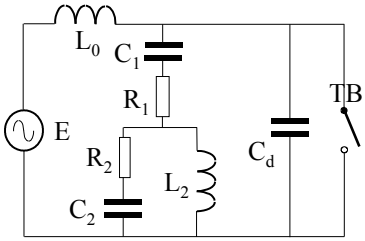


Fig. 145.S

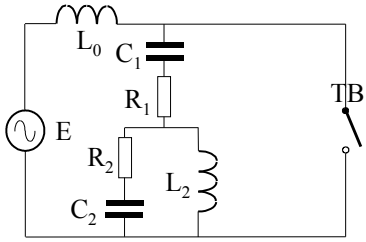
Chapter 2: Test Circuits and CB-Parameters.

Case A: Direct Circuits by Schavemaker.



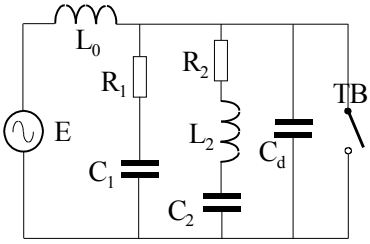
TRV1C

E = 138kV
L_0 = 15.54mH
L_2 = 3.2 mH
C_1 = 0.15 µF
C_2 = 0.315 µF
C_d = 8.88 nF
R_1 = 192.2 Ω
R_2 = 33 Ω



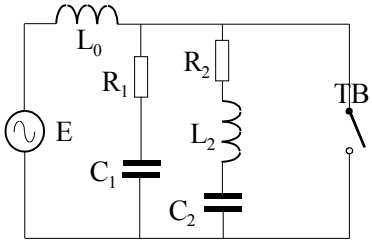
TRV1R

E = 138kV
L_0 = 15.54 mH
L_2 = 3.2 mH
C_1 = 0.11 µF
C_2 = 0.315 µF
R_1 = 117 Ω
R_2 = 33 Ω



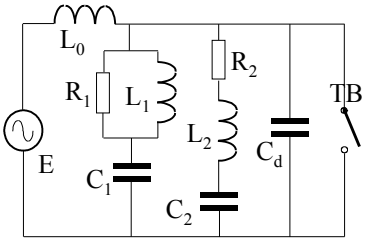
TRV2C

E = 131kV
L_0 = 14.75 mH
L_2 = 27.8 mH
C_1 = 0.083 µF
C_2 = 0.084 µF
C_d = 8.88 nF
R_1 = 225.2 Ω
R_2 = 112.6 Ω



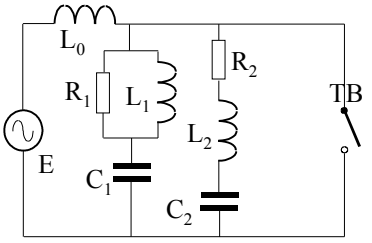
TRV2R

E = 131kV
L_0 = 14.75 mH
L_2 = 27.8 mH
C_1 = 0.075 µF
C_2 = 0.084 µF
R_1 = 150 Ω
R_2 = 112.6 Ω



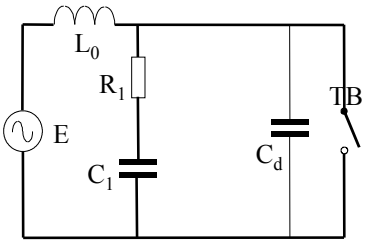
TRV3C

E = 133kV
L_0 = 14.98 mH
L_1 = 9.85 mH
L_2 = 17 mH
C_1 = 0.055 µF
C_2 = 0.14 µF
C_d = 8.88 nF
R_1 = 225.2 Ω
R_2 = 185 Ω



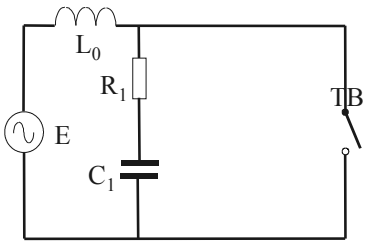
TRV3R

E = 133kV
L_0 = 14.98 mH
L_1 = 9.85 mH
L_2 = 17 mH
C_1 = 0.061 µF
C_2 = 0.14 µF
R_1 = 150 Ω
R_2 = 185 Ω



TRV4C

E = 131kV
L_0 = 14.75 mH
C_1 = 0.11 µF
C_d = 8.88 nF
R_1 = 225.2 Ω



TRV4R

E = 131kV
L_0 = 14.75 mH
C_1 = 0.087 µF
R_1 = 150 Ω

EMTP, Kopplin-parameters;

K_t = 8.5787^E-6, K_p= 3.8756^E+6, [V_{con} = 2000 V]

X-Trans, KEMA-parameters;

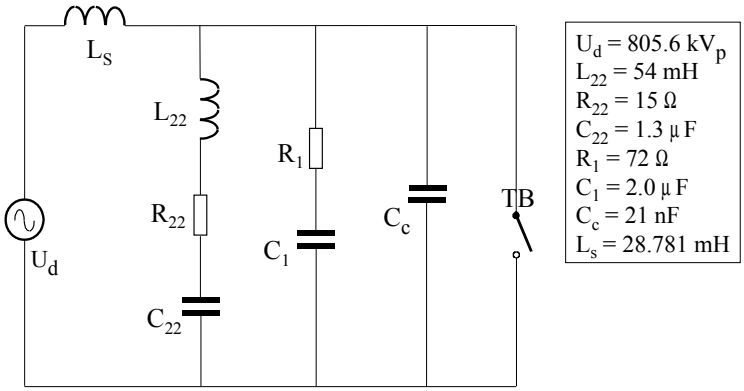
P = 5.5 bar

Mayr-part:	Recombination-part:
P_0 = 500 W/bar	l_a = 5 cm
C_0 = 220 V/bar	$r_a{}^0$ = 1 mm
τ = 1.2 µsec	τ_r = 0.5 msec

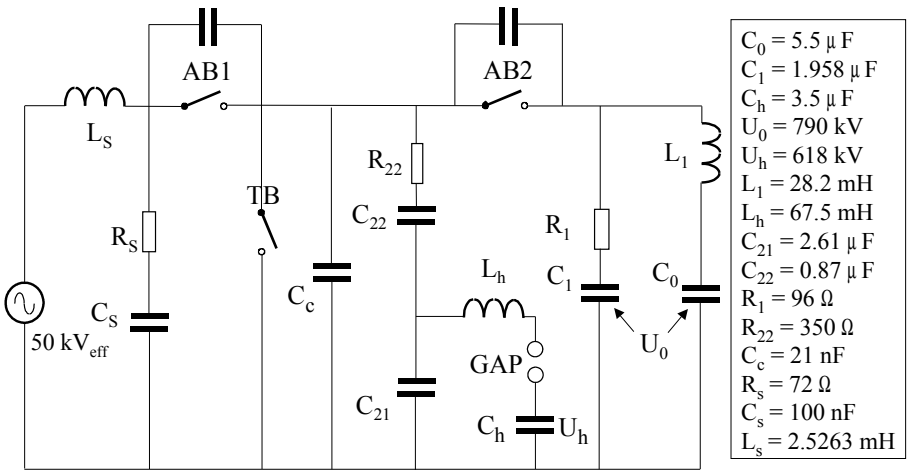
g_0 = 1.0 S

c_d = 0.1 m2bar/kVs
c_e = 1.4^E-20 Am2bar/kV
c_i = 1.4^E-22 Am2bar/kV
α_{eff} = -0.01 1/m
γ = 3000 1/s
β_{e-i} = 3.0^E-14 m3/s
β_{i-i} = 5.0^E-13 m3/s
$(E/N)_{crit}$ = 4.5^E+5 Vm2

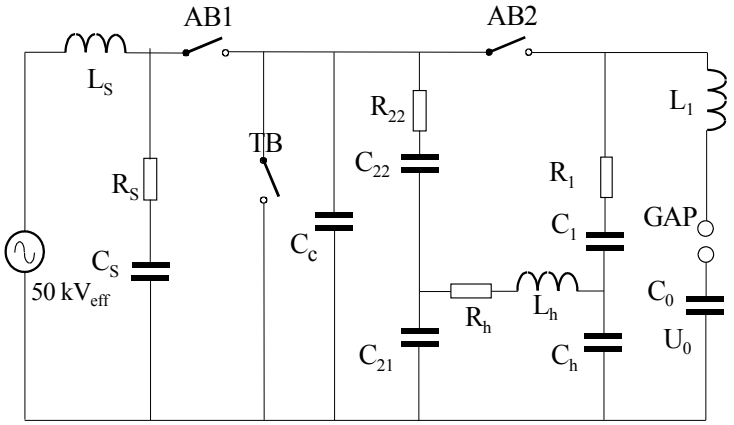
Case B: UHV Circuits compared by Sheng.



Reference Direct Circuit

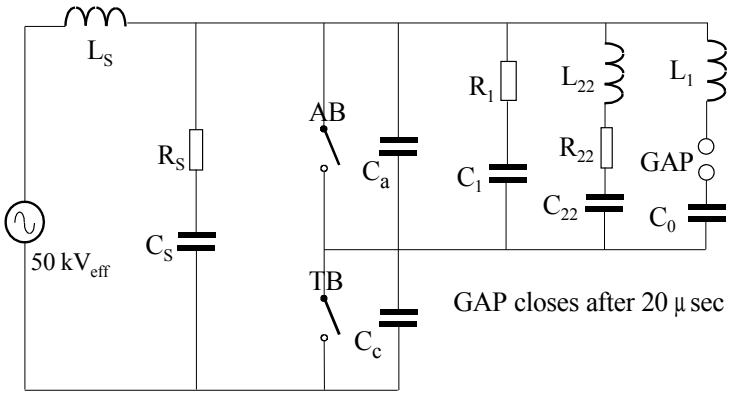


Enhanced Parallel Injection Circuit



$C_0 = 6.0\ \mu F$
$C_h = 6.171\ \mu F$
$C_1 = 4.8\ \mu F$
$U_0 = 812$ kV
$L_1 = 29.0$ mH
$L_h = 178$ mH
$C_{21} = 0.45\ \mu F$
$C_{22} = 0.055\ \mu F$
$R_1 = 85.8\ \Omega$
$R_h = 81.2\ \Omega$
$R_{22} = 49.2\ \Omega$
$C_c = 21$ nF
$R_s = 72\ \Omega$
$C_s = 100$ nF
$L_s = 2.5263$ mH

Hitachi Circuit



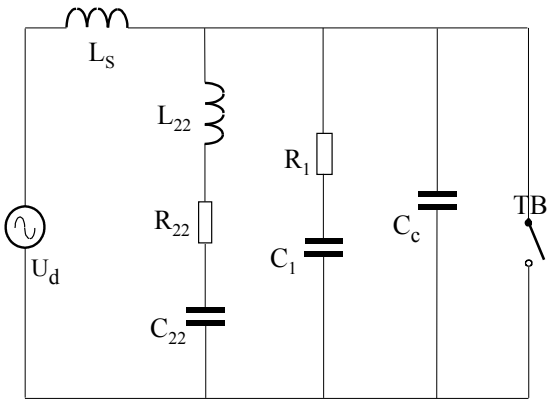
$C_0 = 3.6\ \mu F$
$U_0 = 990$ kV
$L_1 = 180$ mH
$L_{22} = 160$ mH
$R_{22} = 350\ \Omega$
$C_{22} = 0.47\ \mu F$
$R_1 = 450\ \Omega$
$C_1 = 0.35\ \mu F$
$C_a = 100$ nF
$C_c = 15$ nF
$R_s = 72\ \Omega$
$C_s = 100$ nF
$L_s = 2.5263$ mH

Voltage Injection Circuit

EMTP, Kopplin-parameters;

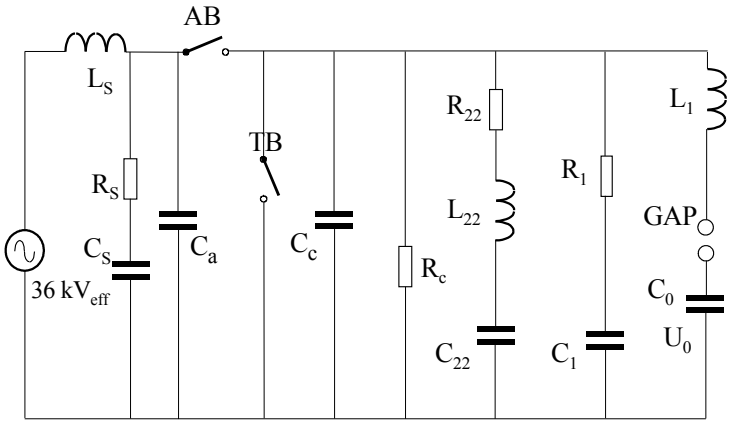
$K_t = 3.5^E-6$, $K_p = 7.0^E+6$, [$V_{con} = 2400$ V]

Case C: Circuits compared by vd Sluis and Rutgers.



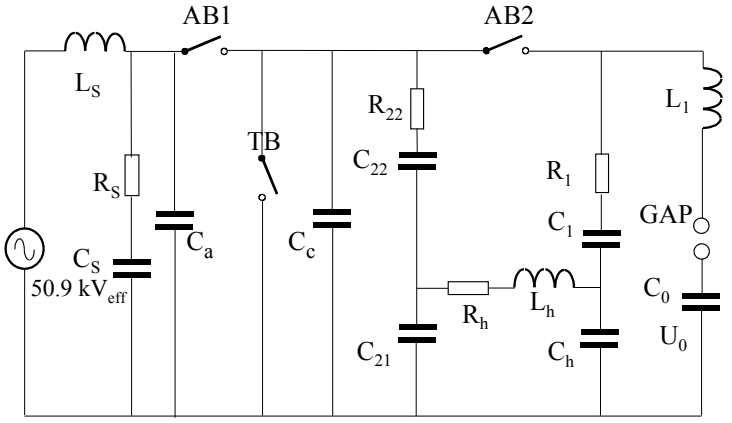
$U_d = 260.2\ kV_p$
$L_{22} = 23$ mH
$R_{22} = 45\ \Omega$
$C_{22} = 0.4\ \mu F$
$R_1 = 94\ \Omega$
$C_1 = 0.5\ \mu F$
$C_c = 21$ nF
$L_s = 12.2$ mH

Reference Direct Circuit



$C_0 = 10.7\ \mu F$
$U_0 = 286$ kV
$L_1 = 13.4$ mH
$L_{22} = 19.5$ mH
$C_{22} = 0.5\ \mu F$
$R_{22} = 56\ \Omega$
$C_1 = 0.5\ \mu F$
$R_1 = 94\ \Omega$
$C_a = 100$ nF
$C_c = 21$ nF
$R_c = 13$ kΩ
$R_s = 94\ \Omega$
$C_s = 0.5\ \mu F$
$L_s = 2.38$ mH

Weil-Dobke Circuit



$C_0 = 6.67\ \mu F$
$C_h = 2.47\ \mu F$
$C_1 = 1.54 \mu F$
$U_0 = 256$ kV
$L_1 = 11.3$ mH
$L_h = 20.2$ mH
$C_{21} = 0.45\ \mu F$
$C_{22} = 0.055\ \mu F$
$R_1 = 104\ \Omega$
$R_h = 56.8\ \Omega$
$R_{22} = 207\ \Omega$
$C_c = 100$ pF
$C_a = 0.32\ \mu F$
$R_s = 91\ \Omega$
$C_s = 0.95\ \mu F$
$L_s = 3.31$ mH

Hitachi Circuit

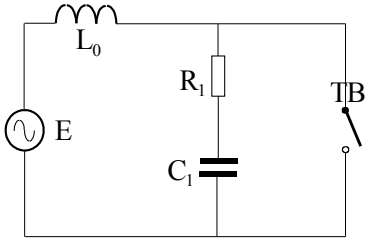
EMTP, Urbanek-parameters SF6-breaker;

ϑ = 5.0^{E}-6, P_0 = 7.0^{E}+4, ud = 100 kV, e = 1500 V [V_{con} = 1450 V]

EMTP, Kopplin-parameters Air-breaker;

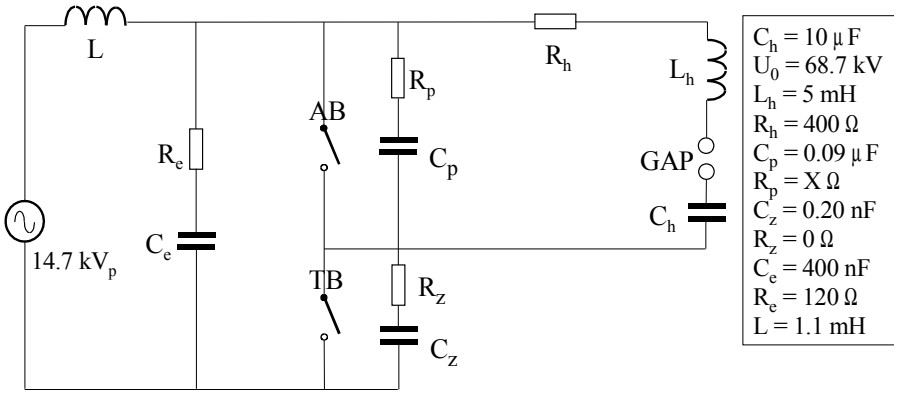
K_t = 40.0^{E}-6, K_p= 175.0^{E}+6, [V_{con} = 5000 V]

Case D: Circuits investigated by Blahous.



E = 58.8kV
L_0 = 4.4 mH
C_1 = 0.38 µF
R_1 = 100 Ω

Reference Direct Circuit



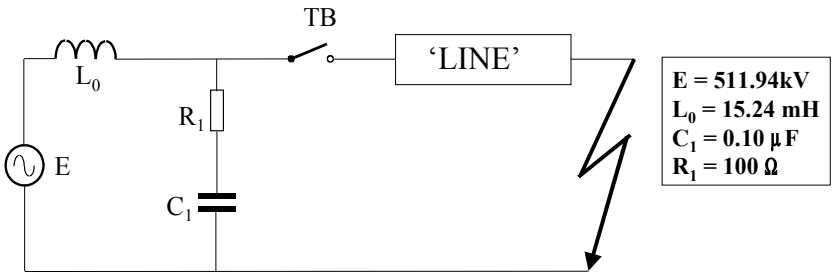
Synthetic Test Circuit

X-Trans, KEMA-parameters (for both TB and AB);

P = 5.0 bar

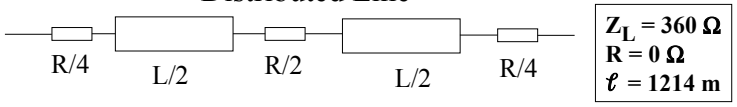
Mayr-part:	Recombination-part:
P_0 = 5000 W/bar	l_a = 5 cm
C_0 = 100 V/bar	r_a^0 = 1 mm
τ = 1.2 µsec	τ_r = 0.5 msec
g_0 = 10.0 S	c_d = 0.1 m2bar/kVs
	c_e = 1.4E-20 Am2bar/kV
	c_i = 1.4E-22 Am2bar/kV
	α_{eff} = -0.1 1/m
	γ = 3000 1/s
	β_{e-i} = 3.0E-15 m3/s
	β_{i-i} = 5.0E-14 m3/s
	$(E/N)_{crit}$ = 5.0E+5 Vm2

Case E: SLF-Circuits investigated by Guy St-Jean.

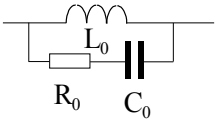


Direct SLF Circuit

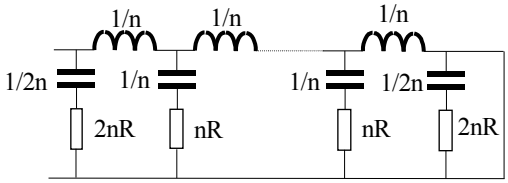
Distributed Line



RLC-circuit

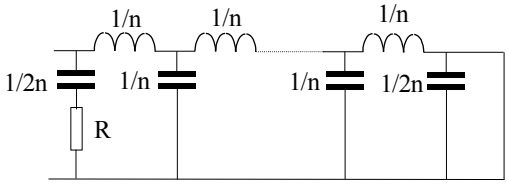


L_0 = 1.6xL
L_0 = 2.4113 mH
C_0 =0.0116283 µF
R_0 = 360 Ω



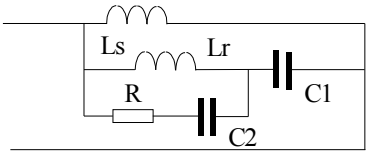
nπ#3-circuit

Z = 360 Ω
n = 8
R = 0.9 Z
L/n = 0.1883824 mH
C/n =1.4535 nF
nR =2592 Ω



nπ#4-circuit

Z = 360 Ω
n = 8
L/n = 0.1883824 mH
C/n =1.4535 nF
R =360 Ω



KEMA 1.7-circuit

R = 360 Ω
Ls = 1.50706 mH
Lr = 0.37676 mH
C1 = 3.87618 µF
C2 = 3.87618 µF

EMTP, Urbanek-parameters SF6-breaker;

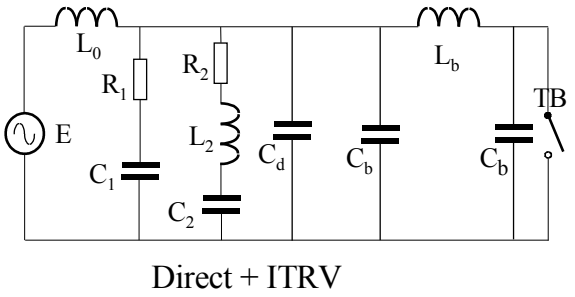
ϑ = 1.0^E-6, P_0 = 3.0^E+5, ud = 400 kV, e = 7500 V [V_{con} = 7500 V]

X-Trans, KEMA-parameters;

P = 9.0 bar

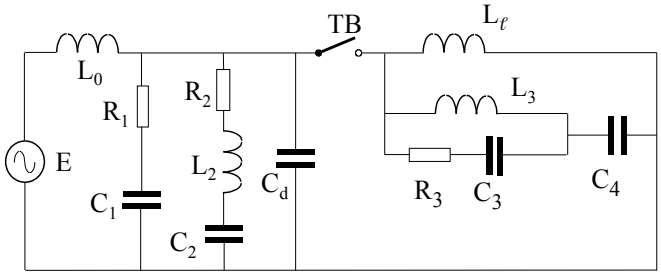
Mayr-part:	Recombination-part:
P_0 = 40000 W/bar	l_a = 5 cm
C_0 = 300 V/bar	r_a^0 = 1 mm
τ = 0.5 µsec	τ_r = 0.5 msec
g_0 = 100.0 S	c_d = 0.1 m2bar/kVs
	c_e = 1.4^E-20 Am2bar/kV
	c_i = 1.4^E-22 Am2bar/kV
	α_{eff} = -0.01 1/m
	γ = 3000 1/s
	β_{e-i} = 5.0^E-15 m3/s
	β_{i-i} = 5.0^E-14 m3/s
	$(E/N)_{crit}$ = 1.0^E+10 Vm2

Case F: ITRV and SLF phenomena.



Direct + ITRV

E = 260.22kV
L_0 = 12.2 mH
L_2 = 23 mH
C_1 = 0.5 µ F
C_2 = 0.4 µ F
C_d = 21 nF
R_1 = 94 Ω
R_2 = 45 Ω
L_b = 0.078 mH
C_b = 0.5769 nF

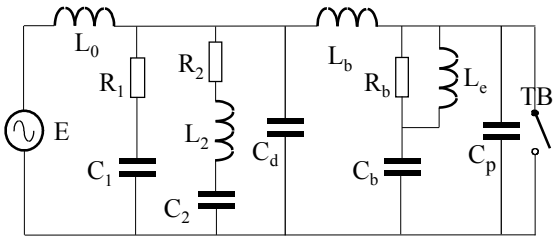


Direct + SLF

E = 260.22kV
L_0 = 12.2 mH
L_2 = 23 mH
C_1 = 0.5 µF
C_2 = 0.4 µF
C_d = 21 nF
R_1 = 94 Ω
R_2 = 45 Ω
R_3 = 450 Ω
$L_ℓ$ = 1.355 mH
L_3 = 0.388 mH
C_3 = C_4 = 1.646 nF

EMTP, Urbanek-parameters SF6-breaker;

ϑ = 5.0E-6, P_0 = 7.0E+5, ud = 100 kV, e = 1500 V [V_{con} = 1450 V]



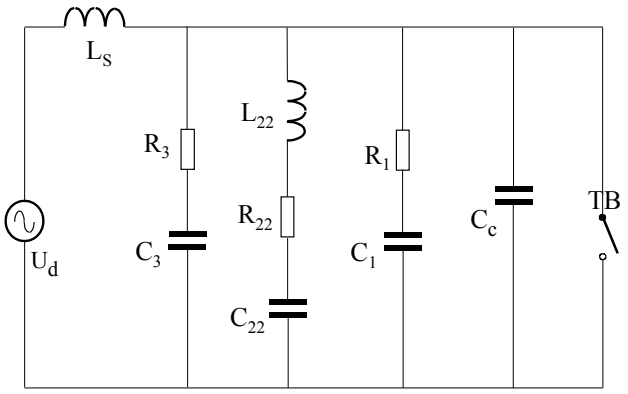
Direct + 'new' ITRV

E = 260.22kV
L_0 = 12.2 mH
L_2 = 23 mH
C_1 = 0.5 µ F
C_2 = 0.4 µ F
C_d = 21 nF
R_1 = 94 Ω
R_2 = 45 Ω
L_b = 0.090 mH
L_e = 0.0045mH
R_b = 260 Ω
C_b = 532.5 pF
C_p = 100 pF

EMTP, Urbanek-parameters modified SF6-breaker;

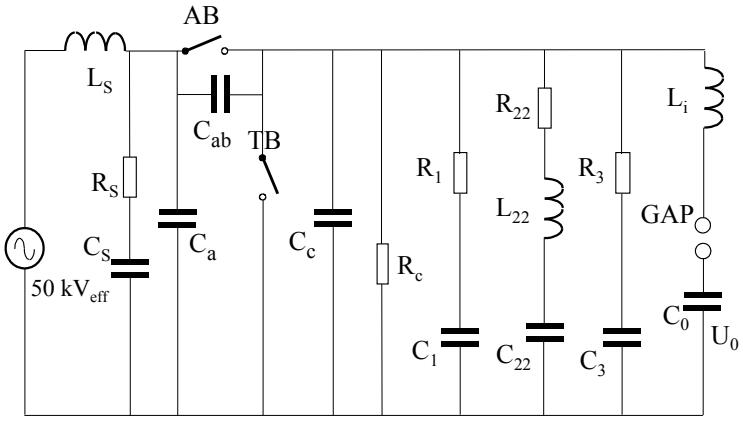
ϑ = 4.5E-6, P_0 = 7.0E+5, ud = 100 kV, e = 1500 V [V_{con} = 1450 V]

Case G: Analysis of Weil-Dobke Circuit.
Trigger-moment and variation of RFC (di/dt).



U_d = 240 kV_p
L_s = 10.804 mH
R_3 = 28 Ω
C_3 = 2.9 µF
L_{22} = 13.47 mH
R_{22} = 14 Ω
C_{22} = 2.32 µF
R_1 = 33 Ω
C_1 = 0.14 µF
C_c = 200 nF

Reference Direct Circuit



C_0 = 21.3 µF
U_0 = 278.5 kV
L_i = 12.54 mH
C_3 = 2.25 µF
R_3 = 33 Ω
L_{22} = 12 mH
C_{22} = 2.25 µF
R_{22} = 0 Ω
C_1 = 0.1 µF
R_1 = 33 Ω
C_{ab} = 100 nF
C_a = 200 nF
C_c = 0.17 µF
R_c = 8 kΩ
R_s = 25 Ω
C_s = 3.2 µF
L_s = 3.18 mH

Weil-Dobke Circuit

EMTP, Urbanek-parameters SF6-breaker;

ϑ = 4.0^{E}-6, P_0 = 2.0^{E}+4, ud = 250 kV, e = 1500 V [V_{con} = 1450 V]

For the analysis of the injection frequency: the tool, the circuits and SF6 CB-parameters of case C were used.

APPENDIX II

Chapter 5: Historical Three-phase Circuits.

Circuit proposed by Bitsch et al.

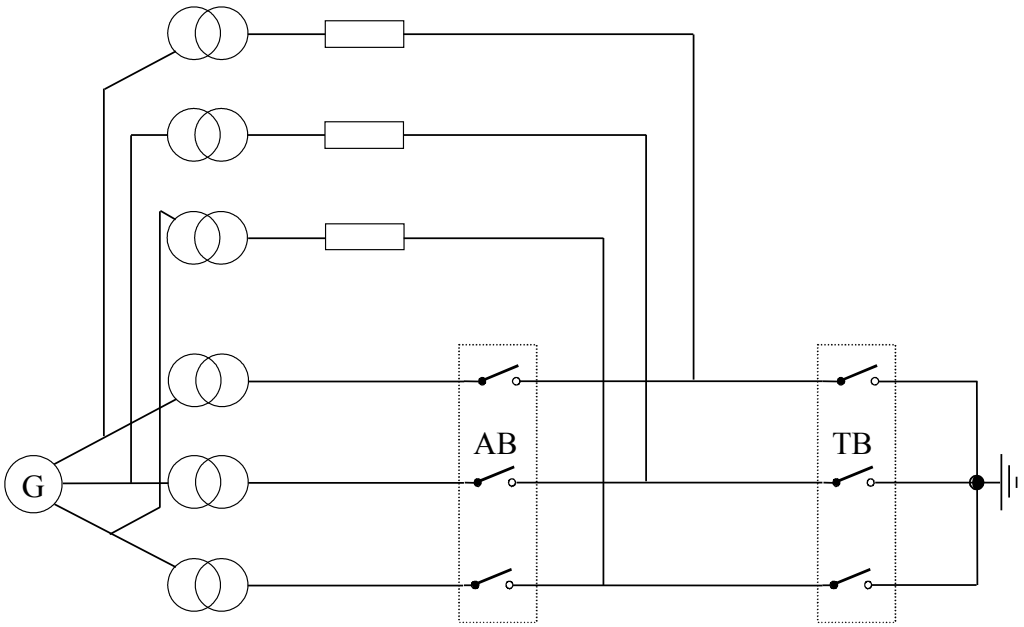


Fig. A

Circuit proposed by Damstra and Kempen.

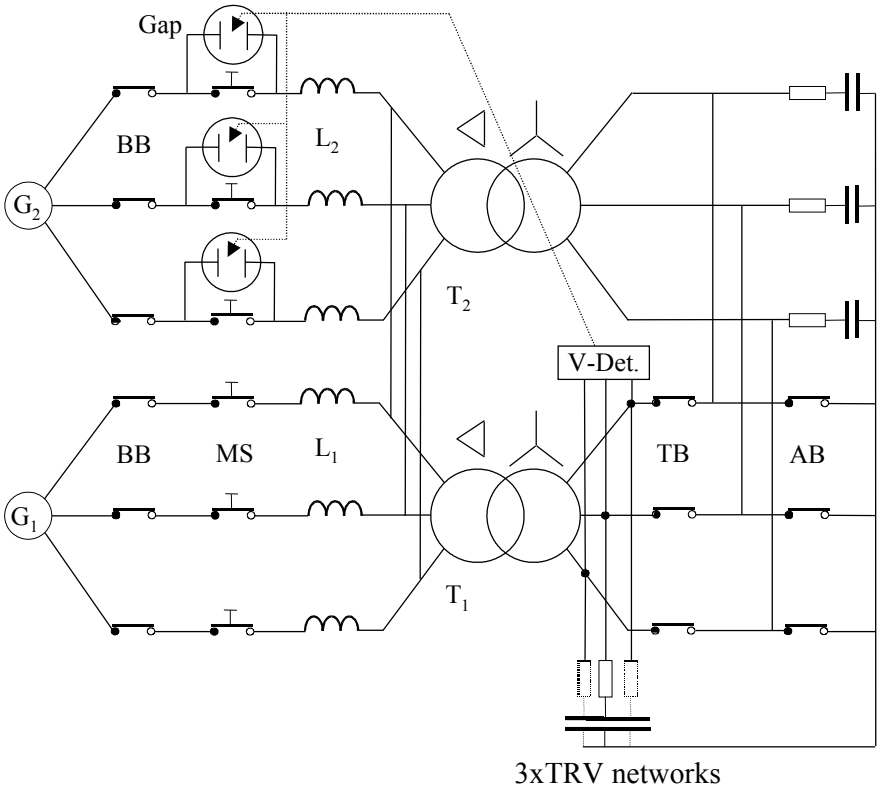


Fig. B

Circuit proposed by Azumi et al.

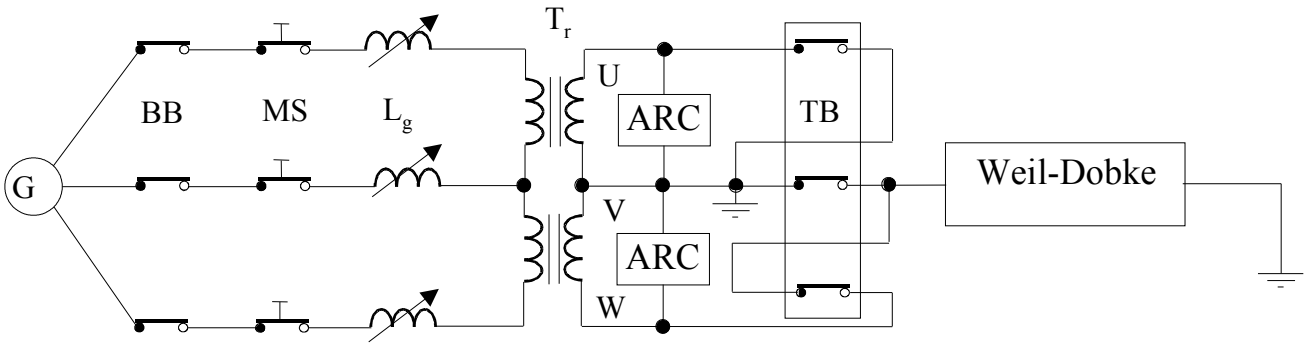


Fig. C

Circuit proposed by Manganaro (CESI).

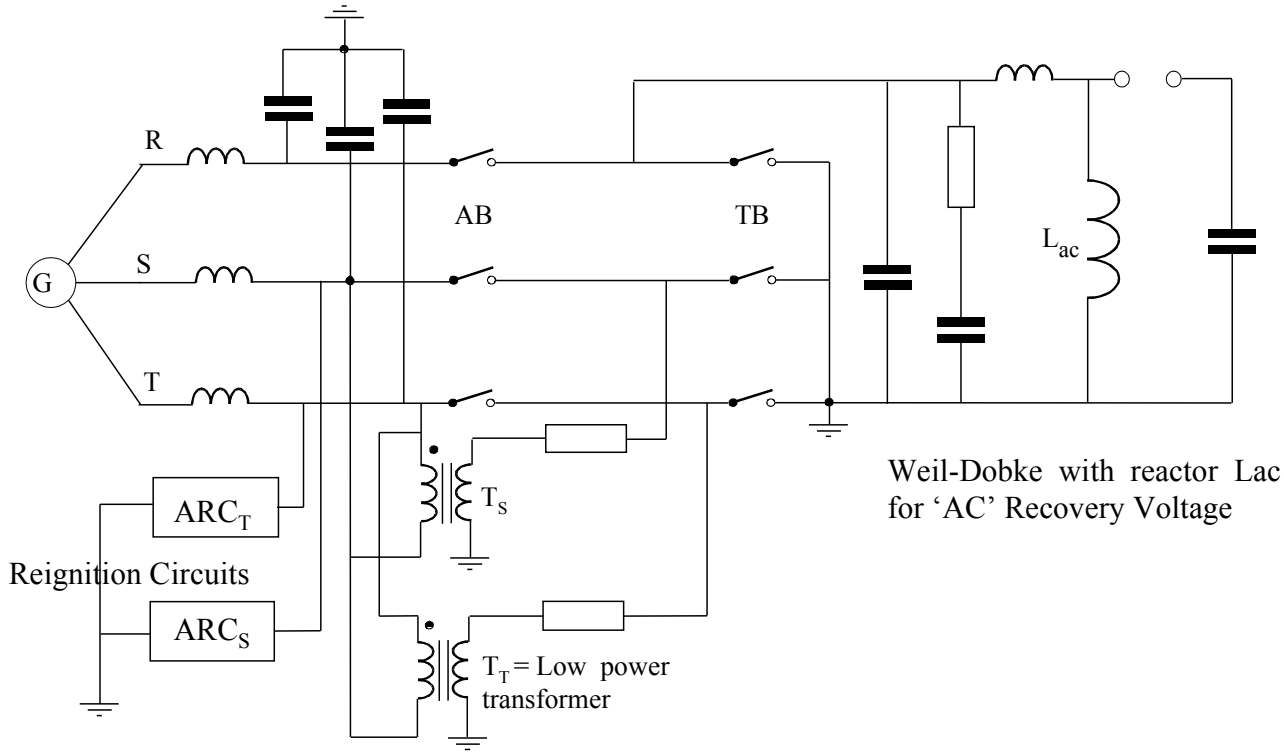


Fig. D

Circuit proposed by Nakanishi et al.

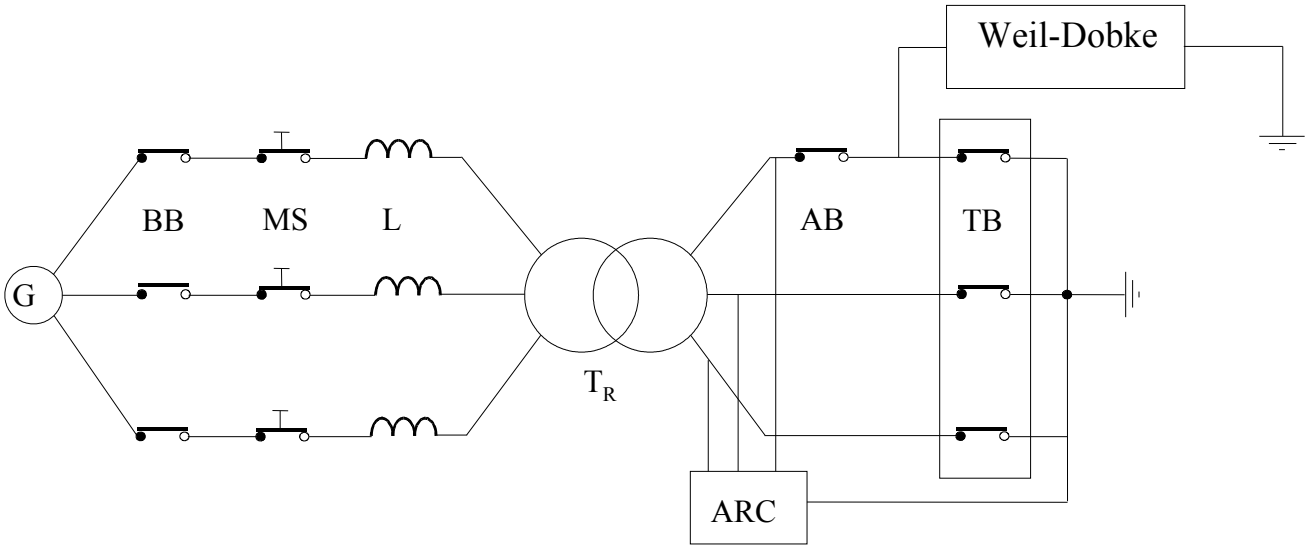


Fig. F

Circuit proposed by Yamamoto et al.

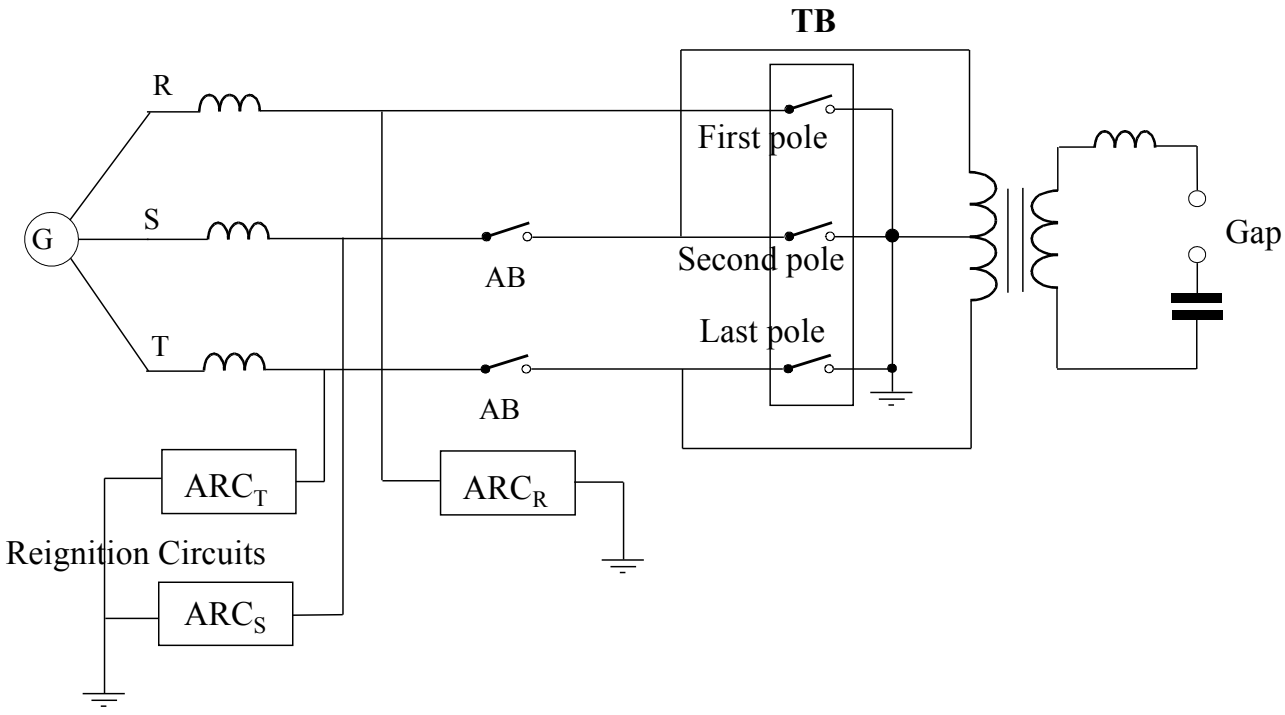


Fig. G

Circuit proposed by van der Linden and van der Sluis.

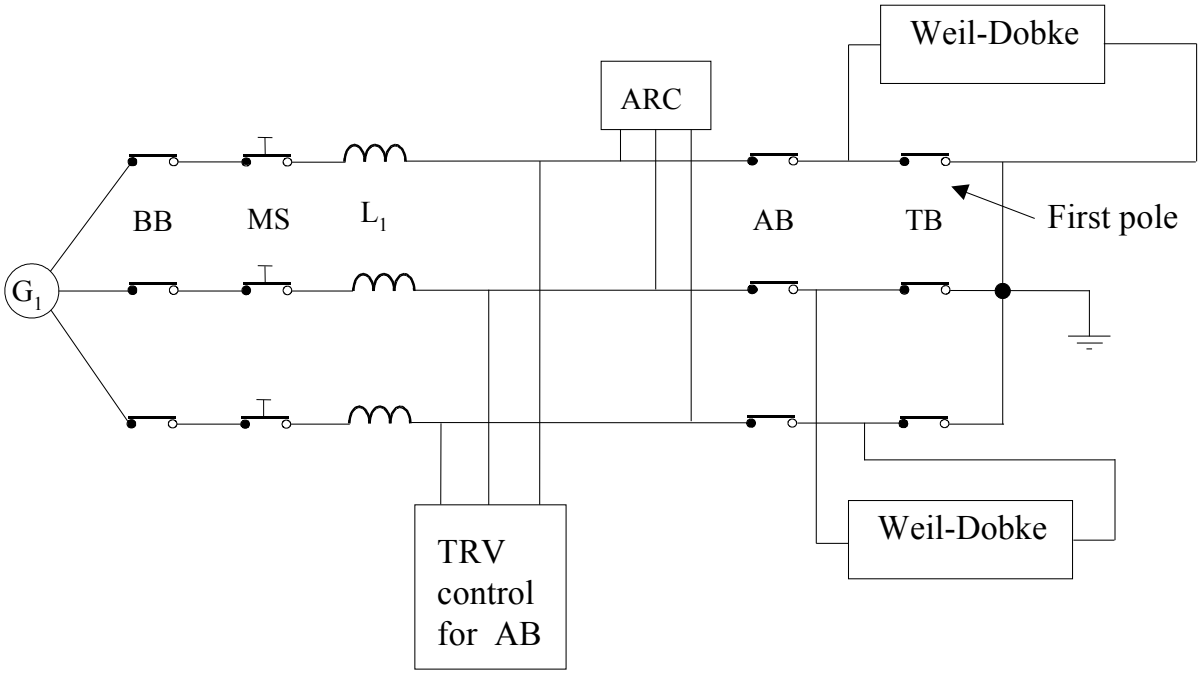


Fig. H

Circuit proposed by Froehlich et al.

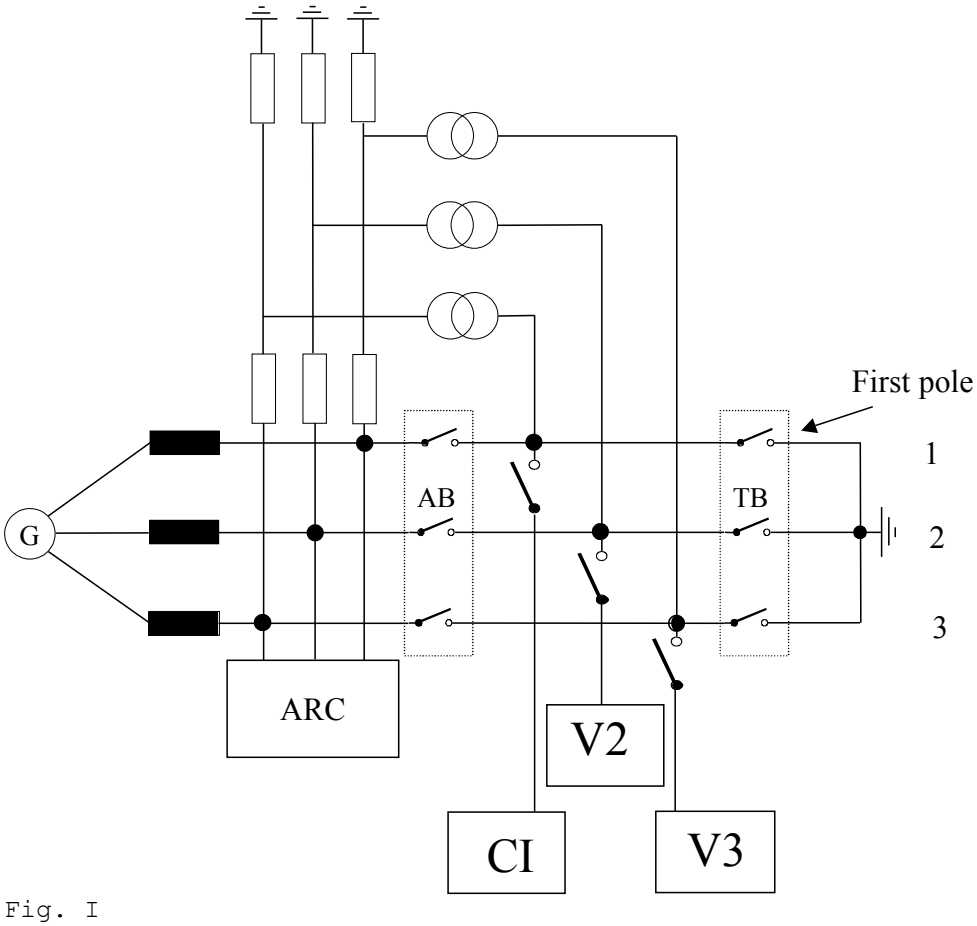


Fig. I

Circuit proposed by Yamashita et al.

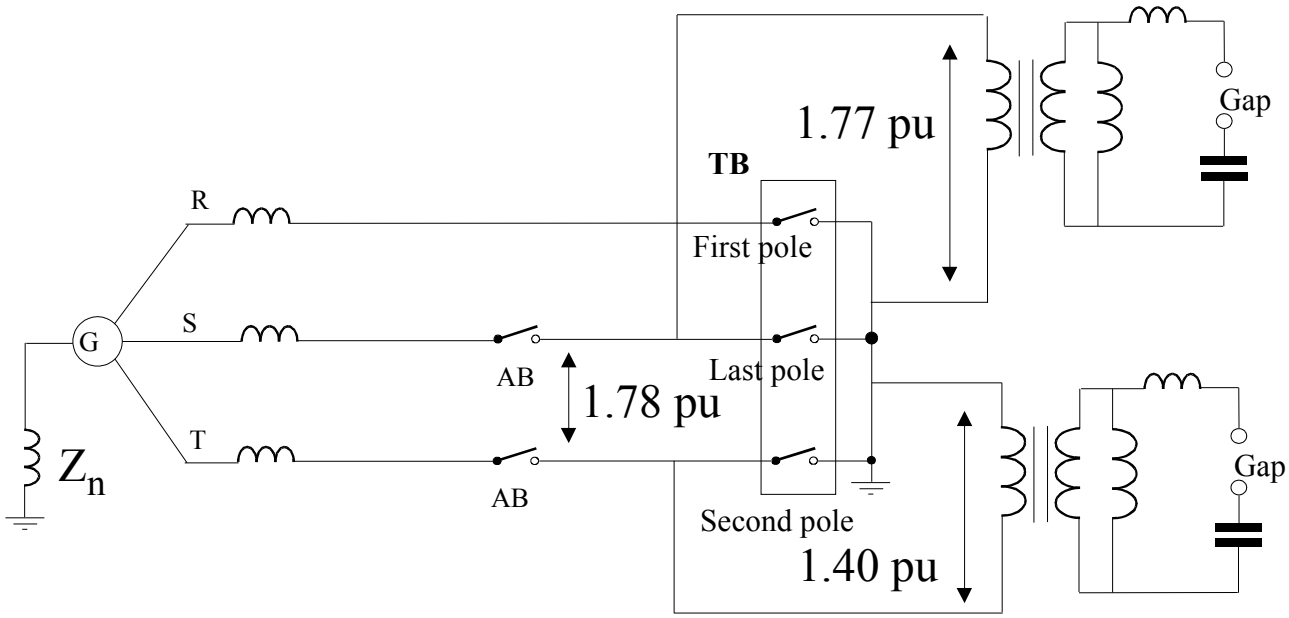


Fig. K

Acknowledgements

First and foremost I wish to thank Lou van der Sluis for accepting my idea of doing a Ph.D research as a Houseman.
It was Lou who introduced me to the subject and although there were times we had to model our interaction as to be able to set its 'severity' to a certain level (like Epa), I really enjoyed the time spent at the Power Systems Laboratory at Delft University.

Therefore I also wish to thank all members of this group for their cooperation but I would like to thank Pieter Schavemaker in particular for his magical mathematical abilities and many discussions which at times were badly needed.

Of the people of the KEMA I wish to thank Rene Smeets for his unwaivering support even at times when he had to read some unreadable stuff.
By doing so he was the single source of inspiration to continue.
And I wish to thank Wim van der Linden for sharing his many years of practical experience.

Over the years I had many discussions with dr. Cliteur, prof. Damstra, prof. Haginomori, ir. Kempen, prof. Kertész, prof. Pannicke, prof. Rutgers and dr. Trapp and I wish to thank them all for helping me understand the intriguing problems of high voltage circuit breaker testing.

Furthermore I have to thank mrs. Hans Pielkenrood who worked her way through the manuscript more than once and succeeded in producing a readable text throughout.

Last but not least I am indebted to my wife Monique and our two children Anne and Pieter for their endurance through moments of emotional stress when things did not work the way I wanted them to.

Curriculum Vitae

Name: Adriaan Johannes Pieter de Lange
October 21, 1957 in Alkmaar, the Netherlands.

Adriaan was born as the eldest son of drs. Pieter de Lange and Barbara Lucresa Kern.

He went to primary school in The Hague and Bloemendaal from 1964 until 1970 and to High School at the Atheneum-department of the Lorentz-scholengemeenschap in Haarlem from 1970 until 1977.

In 1977 Adriaan started at Delft University at the department of electrical engineering. He received his degree in 1986 on a thesis:
"a digital differential protection for a double circuit overhead line"
under the supervision of prof. ir. J. de Haas.

During the time at Delft University he did not only study but he also had time to meet Monique van Duijne and get married (1984) and to set up Heracles, a private enterprise (1981/1985).

In 1986 conscription could not be postponed any longer and after having sold Heracles (to his brother Jan) Adriaan served as an army officer at the building department DGW&T of the Royal Dutch Army.

In 1988 Adriaan started his professional career.
To get to the bottom of things his first job was as a mechanic and tester with Rietschoten&Houwens. The second job was as an electrical engineer with Comprimo and the third job as a sales & project engineer and finally project manager with Siemens/KWU.

The work at Siemens, including the work in Germany ('90/'91 in Erlangen and '92/'93 Offenbach), was mainly in the field of building power plants.

In the summer of 1996, after having looked after the children (Anne 1989 and Pieter 1991) for six years, Monique wanted to resume her professional career. She rejoined the Makelaars Associatie, the enterprise which she now partly owns together with her brother Peter and a third partner.

Adriaan wanted to look after the children and next to running the household he started a Ph.D.-research at Delft University department of electrical engineering under the auspices of prof. ir. L. van der Sluis.

The subject of research was new but by helping in writing a book on electrical transients Adriaan was able to lay the cornerstone for the real work.

As from June 1999 Adriaan has resumed his professional career with a full time job and a (practically) finished part-time MBA.